PROGRAMMABLE DMA CONTROLLER - INTEL 8257

- **It is a device to transfer the data directly between IO device and memory without through the CPU. So it performs a high-speed data transfer between memory and I/O device.**

Features

- **The 8257 has four channels and so it can be used to provide DMA to four I/O devices**
- **Each channel can be independently programmable to transfer up to 64kb of data by DMA.**
- **Each channel can be independently perform read transfer, write transfer and verify transfer.**

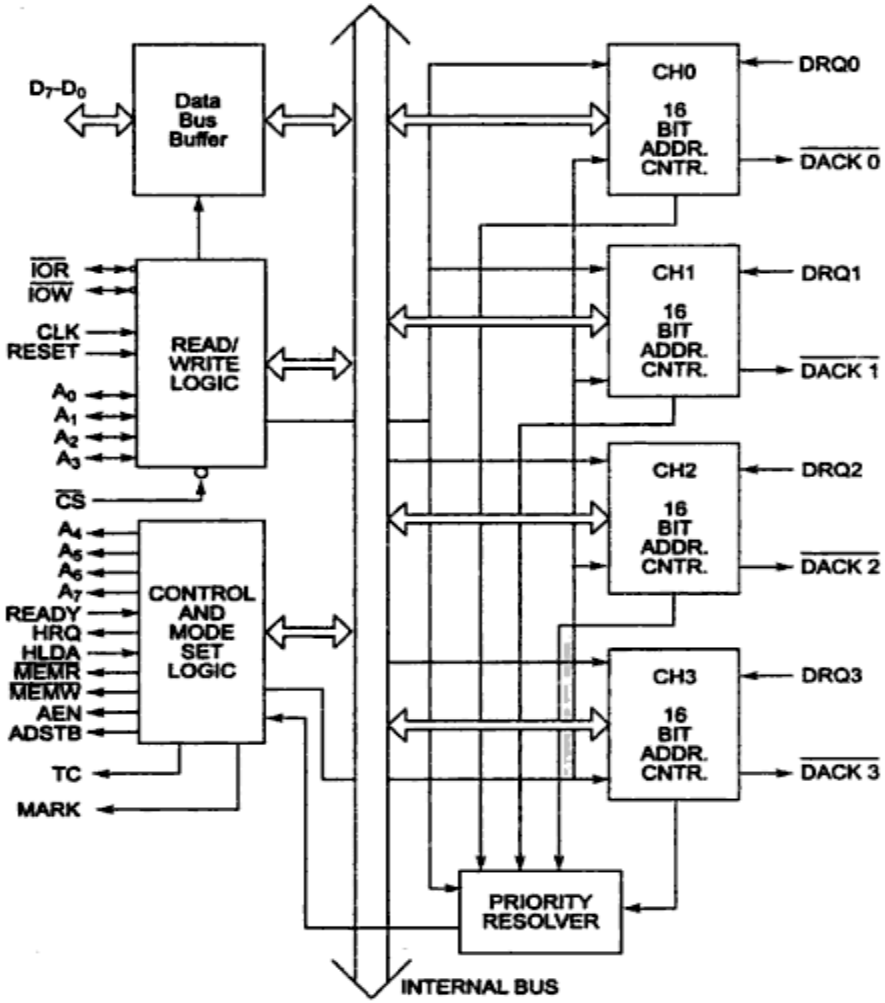


Fig. 7.1 *Internal Architecture of 8257*

Register Organization of 8257

1. DMA Address Register
2. Count Register

X 4

3. Mode Set Register
4. Status Register

Common

Total = 10

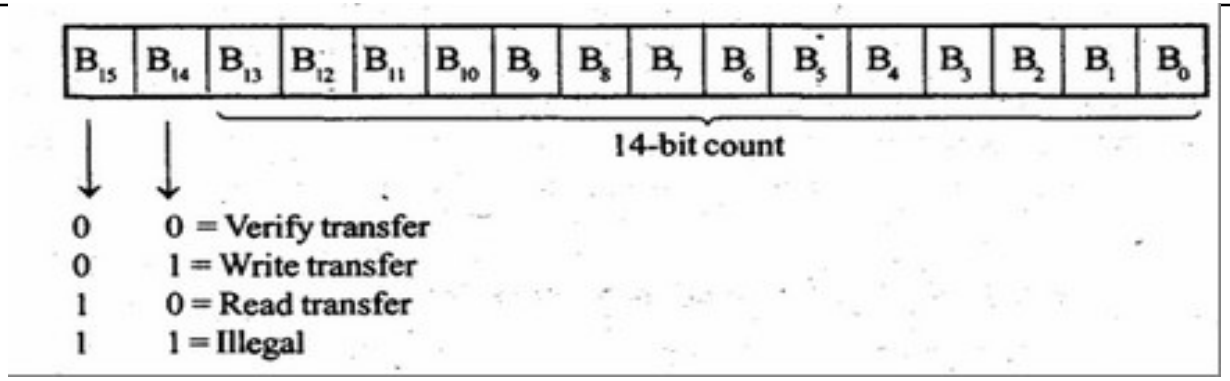
Each channel of 8257 Block diagram has two programmable 16-bit registers named as *address register* and *count register.*

Address register is used to store the starting address of memory location for DMA data transfer.

The address in the address register is automatically incremented after every read/write/verify transfer.

The count register is used to count the number of byte or word transferred by DMA.

Count Register



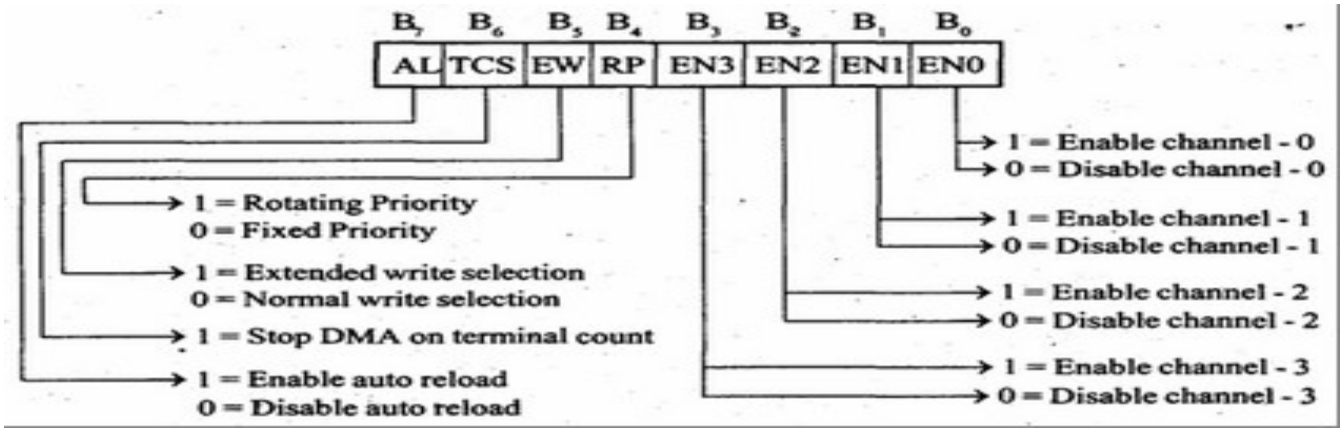
14-bits B0-B13 is used to count value and a 2-bits is used for indicate the type of DMA transfer (Read/Write/Veri1 transfer).

In read transfer the data is transferred from memory to I/O device.

In write transfer the data is transferred from I/O device to memory.

Verification operations generate the DMA addresses without generating the DMA memory and I/O control signals.

Mode Set Register



B0-B3 Enable/disable a channel.
B4 Fixed/rotating priority
B5 Extended / Normal Write time.
B6 Stop DMA on Terminal Count
B7 Auto reloading of channel-2.

If the bit B4 is set to one, then the channels will have rotating priority and if it zero then the channels wilt have fixed priority.

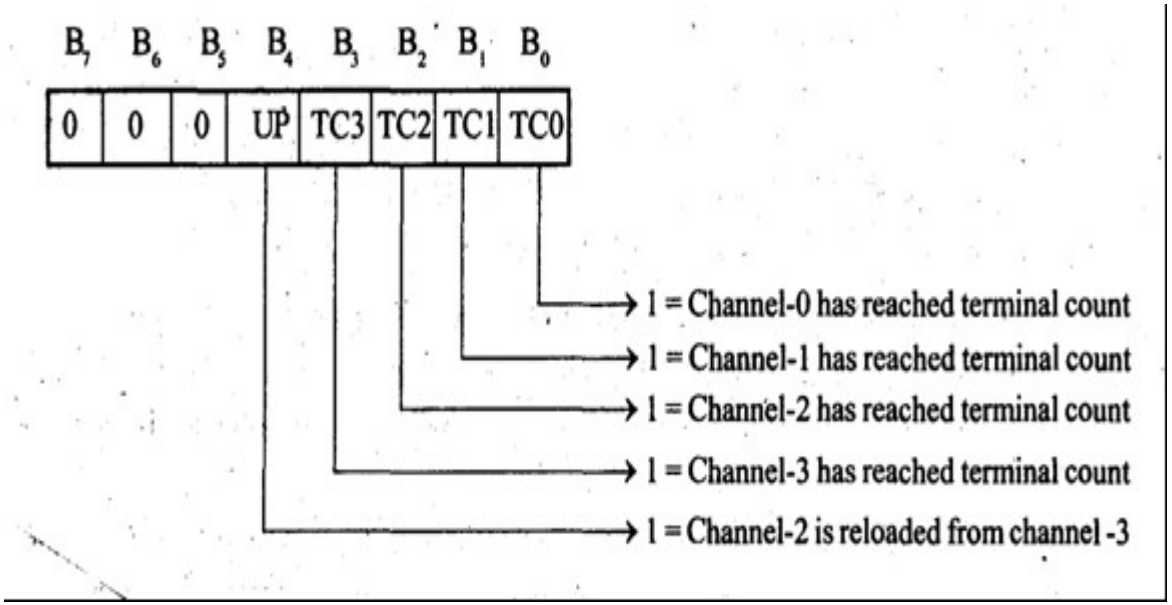
1. In rotating priority after servicing a channel its priority is made as lowest.

2. In fixed priority the channel-0 has highest priority and channel-2 has lowest priority.

The bit B7 is used to select the auto load feature for DMA channel-2.

When bit B7 is set to one, then the content of channel-3 count and address registers are loaded in channel-2 count and address registers respectively whenever the channel-2 reaches terminal count. When this mode is activated the number of channels available for DMA reduces from four to three.

Status Register



8257 Register Selection

Register	Binary Address								Hexa Address
	Decoder input and enable				Input to address pins of 8257				
	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
Channel-0 DMA address register	0	1	1	0	0	0	0	0	60
Channel-0 count register	0	1	1	0	0	0	0	1	61
Channel-1 DMA address register	0	1	1	0	0	0	1	0	62
Channel-1 count register	0	1	1	0	0	0	1	1	63
Channel-2 DMA address register	0	1	1	0	0	1	0	0	64
Channel-2 count register	0	1	1	0	0	1	0	1	65
Channel-3 DMA address register	0	1	1	0	0	1	1	0	66
Channel-3 count register	0	1	1	0	0	1	1	1	67
Mode set register (Write only)	0	1	1	0	1	0	0	0	68
Status register (Read only)	0	1	1	0	1	0	0	0	68

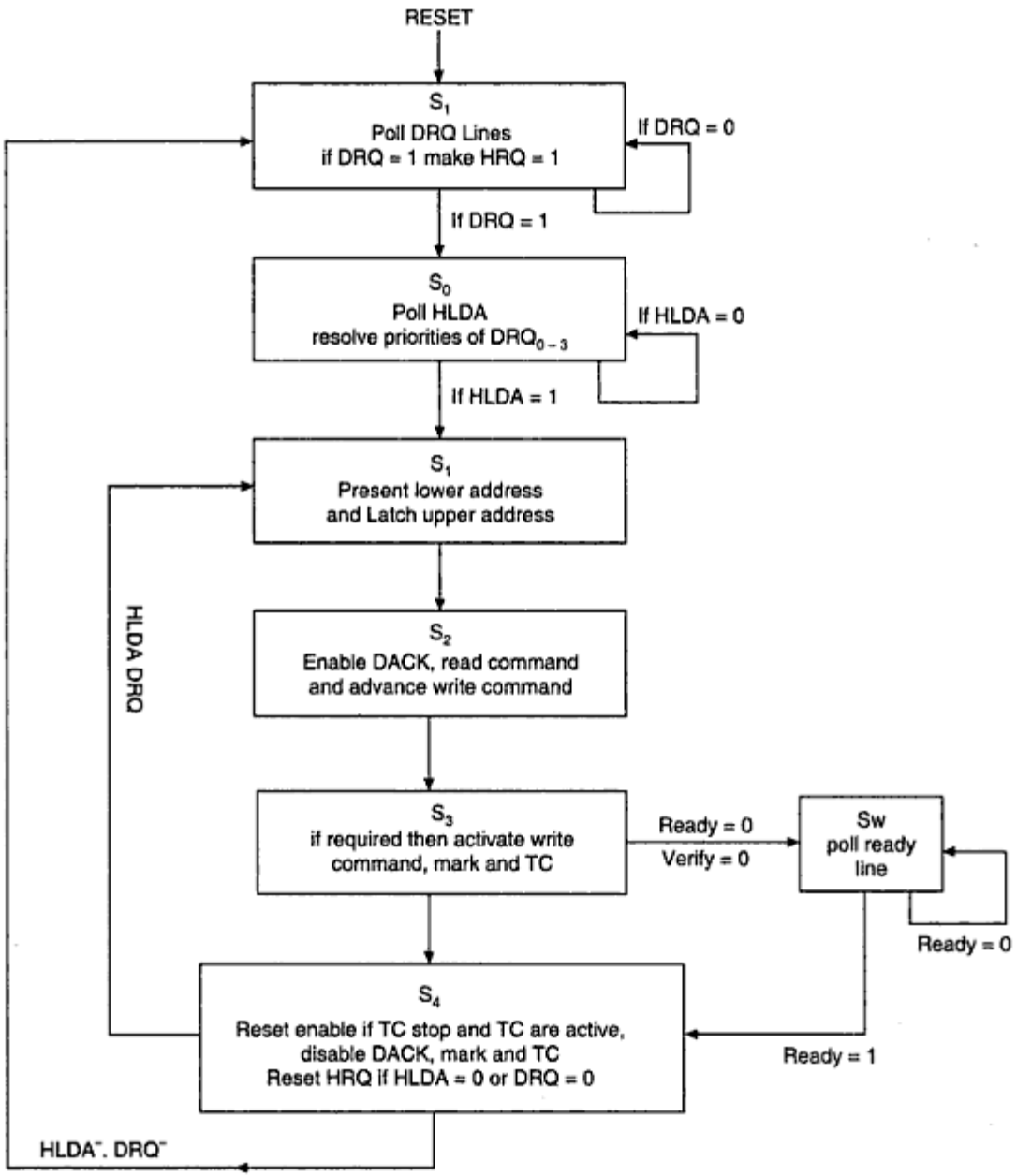


Figure 14.14 State diagram of 8257.

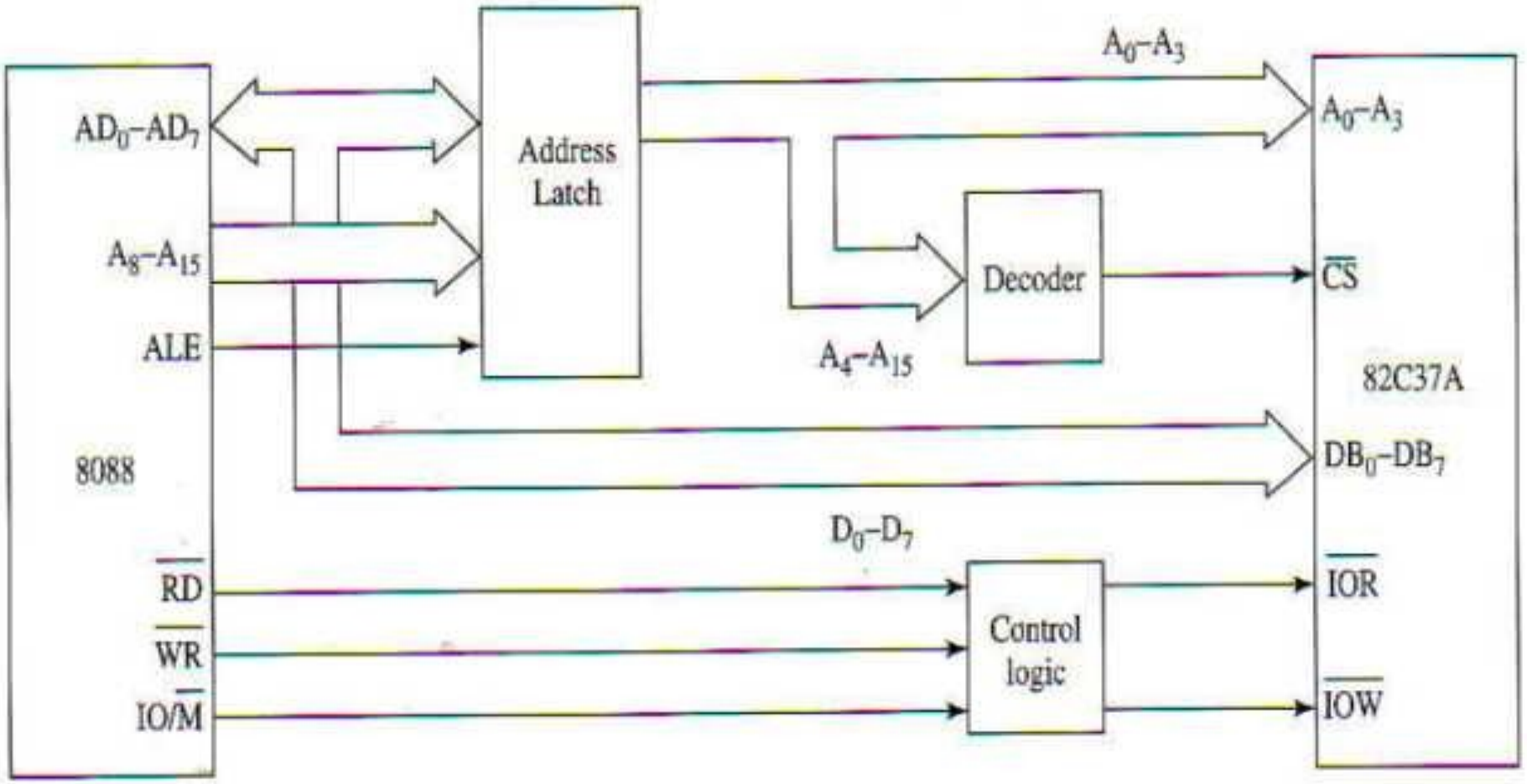
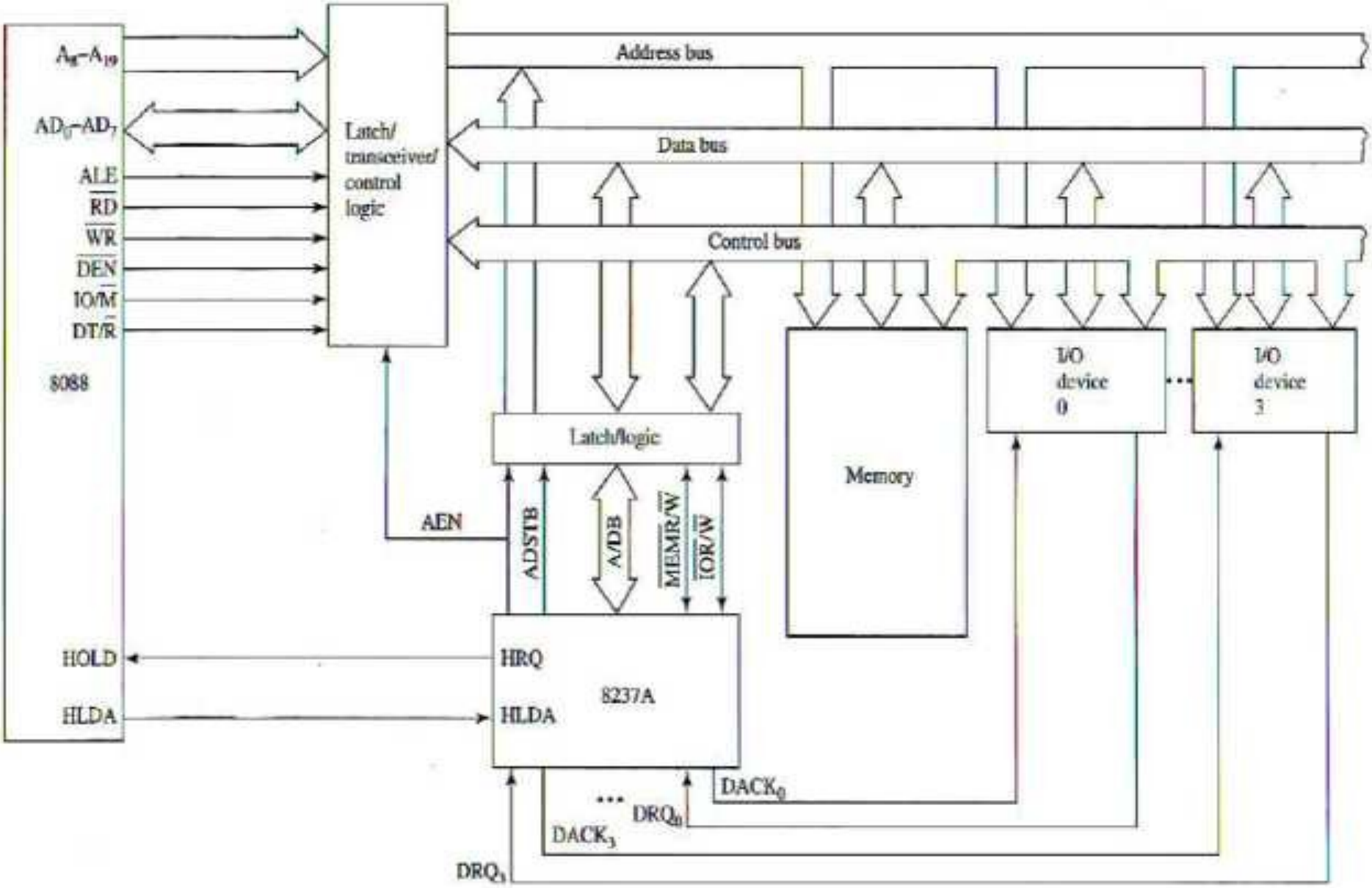


Figure 10–41 Microprocessor interface of 82C37A to the 8088.

DMA interface of the 82C37A



DMA interface of the 82C37A

82C37A contains four independent DMA channels, channel 0 through 3. Typically, each of these channels is dedicated to a specific peripheral device.

In the idle stare. the 82C37A continuously tests these inputs to see if one is active. When a peripheral device wants to perform DMA operations it makes a request for service at its DREQ input by switching it to logic 1.

In response to the active DMA request, the DMA controller switches the hold request (HRQ) output to logic 1.

HLDA of the 8088 is applied to the HLDA input of the 82C37A and signals that the system bus is now available for use by the DMA controller.

82C37A tells the requesting peripheral device that it is ready by outputting a DMA-acknowledge (DACK) signal

During DMA bus cycles, the DMA controller not the MPU, drives the system bus

Atl the beginning of all DMA bus cycles, a 16-bit address is output on lines A_0 through A_7 and DB_0 through DB_7.

The upper 8 bits of the address available on the data bus lines, appear at the same time that address strobe (ADSTB) becomes active

ADSTB is intended to be used to strobe the most significant byte of the address into an external address latch.

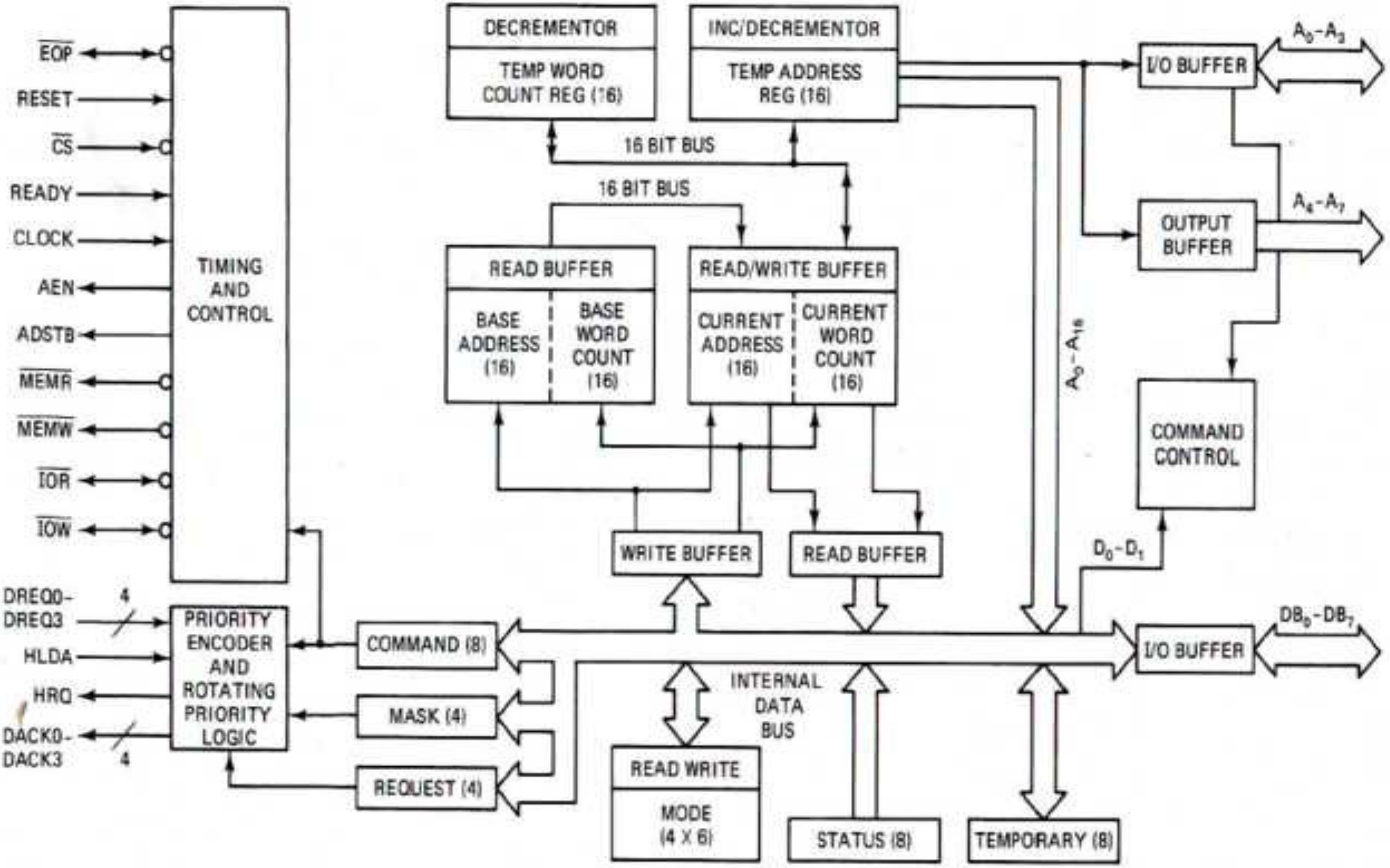
This 16-bit address gives the 82C37A the ability to directly address up to 64Kbytes of storage locations

The address enable (AEN) output signal is active during the complete DMA bus cycle and can be used to both enable the address latch and disable other devices connected to the bus

The 82C37A performs both the memory-to-I/O and I/O-to-memory DMA bus cycles in just four clock periods, while performs memory-to-memory DMA bus Cycles in eight clock periods

The READY input is used to accommodates low memory or I/O devices

Internal Architecture of the 82C37A



Internal Registers of the 82C37A

Timing and control: generates the timing and control signals needed by the external bus interface, it accepts as inputs the READY and CS signals and produces output signals such as ADSTB and AEN.

Priority encoder and rotating priority logic: recognizes one of two priority schemes that can be selected by the 82C37A under software control: fixed priority and rotating priority.

The command control: decodes the register commands applied to the 82C37 A through the microprocessor interface.

12 different types of registers

Name	Size	Number
Base Address Registers	16 bits	4
Base Word Count Registers	16 bits	4
Current Address Registers	16 bits	4
Current Word Count Registers	16 bits	4
Temporary Address Register	16 bits	1
Temporary Word Count Register	16 bits	1
Status Register	8 bits	1
Command Register	8 bits	1
Temporary Register	8 bits	1
Mode Registers	6 bits	4
Mask Register	4 bits	1
Request Register	4 bits	1

Accessing the registers of the 82C37A

Channel(s)	Register	Operation	Register address	Internal FF	Data bus
0	Base and current address	Write	0_{16}	0 1	Low High
	Current address	Read	0_{16}	0 1	Low High
	Base and current count	Write	1_{16}	0 1	Low High
	Current count	Read	1_{16}	0 1	Low High
1	Base and current address	Write	2_{16}	0 1	Low High
	Current address	Read	2_{16}	0 1	Low High
	Base and current count	Write	3_{16}	0 1	Low High
	Current count	Read	3_{16}	0 1	Low High
2	Base and current address	Write	4_{16}	0 1	Low High
	Current address	Read	4_{16}	0 1	Low High
	Base and current count	Write	5_{16}	0 1	Low High
	Current count	Read	5_{16}	0 1	Low High
3	Base and current address	Write	6_{16}	0 1	Low High
	Current address	Read	6_{16}	0 1	Low High
	Base and current count	Write	7_{16}	0 1	Low High
	Current count	Read	7_{16}	0 1	Low High
All	Command register	Write	8_{16}	X	Low
All	Status register	Read	8_{16}	X	Low
All	Request register	Write	9_{16}	X	Low
All	Mask register	Write	A_{16}	X	Low
All	Mode register	Write	B_{16}	X	Low
All	Temporary register	Read	B_{16}	X	Low
All	Clear internal FF	Write	C_{16}	X	Low
All	Master clear	Write	D_{16}	X	Low
All	Clear mask register	Write	E_{16}	X	Low
All	Mask register	Write	F_{16}	X	Low

Each DMA channel has two address registers: the base address register and the current address register, The base address register holds the starting address for the DMA operation, and the current address register contains the address of the next storage location to be accessed.

To load a new 16-bit address into the base register, we must write two separate bytes, one after the other, to the address of the register. The 82C31A has an internal flip-flop called the first/last flip-flop. This flip-flop identifies which byte of the address is being written into the register.

Example: to write the address 1234_{16} in to the base address register and the current address register for channel 0 of a DMA controller located at base I/O address DMA (where DMA is ≤ F0H and it is decided by how the $\overline{CS}$ for the 82C37A must be generated), the following instructions may be executed:

```
MOV  AL, 34H    ;Write low byte
OUT  DMA+0, AL
MOV  AL, 12H    ;Write high byte
OUT  DMA+0, AL
```

This routine assumes that the internal flip-flop was initially set to 0

The 82C37A also has two word count registers for each of its DMA channels: the base count register and the current count register.

These registers are 16 bits in length, and identifies their address as 1_{16} relative to the base address DMA for channel 0.

Actually, the number of bytes transferred is always one more than the value programmed into this register. This is because the end of a DMA cycle is detected by the rollover of the current word count from 0000_{16} to $FFFF_{16}$.

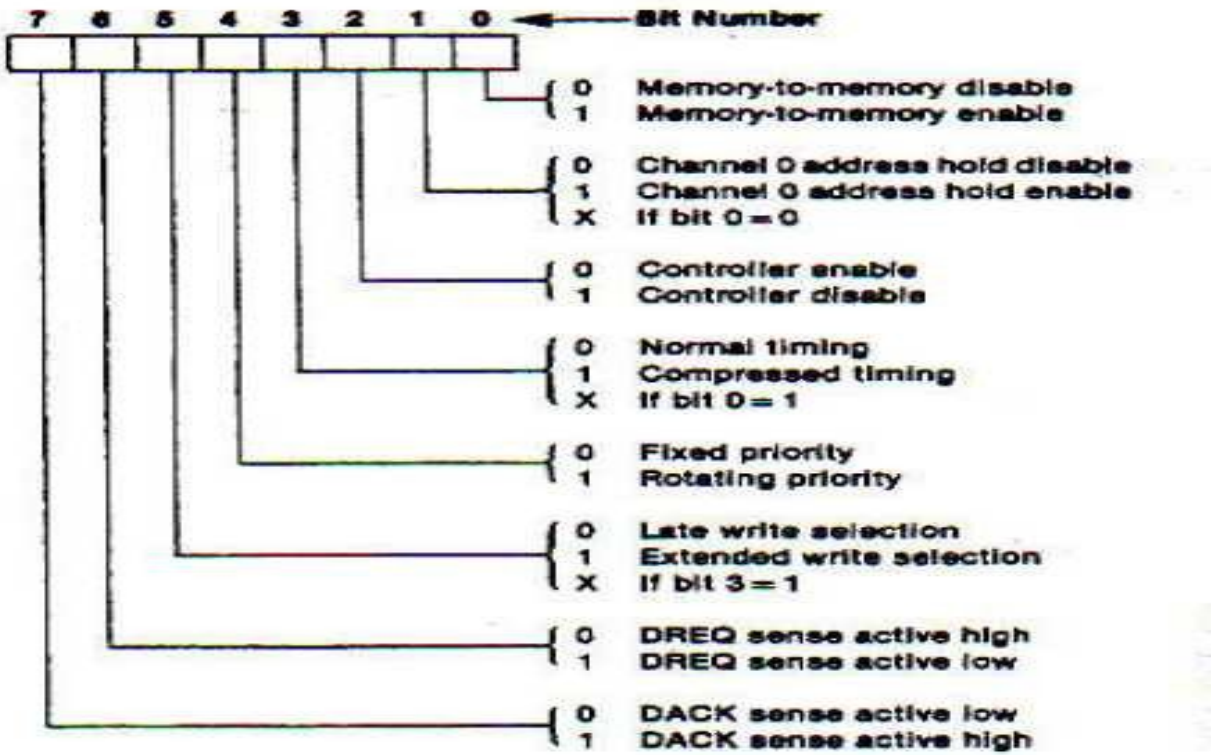
Example: to program a count of $0FFF_{I6}$ into the base and current count registers for channel 1 of a DMA controller located at address DMA (where DMA ≤ F0H), the following instructions can be executed:

```
MOV  AL, 0FFH    ;Write low byte
OUT  DMA+3, AL
MOV  AL, 0FH     ;Write high byte
OUT  DMA+3, AL
```

Again, we have assumed that the internal flip-flop was initially cleared

Command Register

The 8 bits in this register are used to control operating modes that apply to all channels of the DMA controller.



Command Register

EXAMPLE 10.25

If the command register of an 82C37A is loaded with 01_{16}, how does the controller operate?

Solution

Representing the command word as a binary number, we get

$$01_{16} = 00000001_2$$

Referring to Fig. 10–46, we find that the DMA operation can be described as follows:

Bit 0 = 1 = Memory-to-memory transfers are disabled

Bit 1 = 0 = Channel 0 address increments/decrements normally

Bit 2 = 0 = 82C37A is enabled

Bit 3 = 0 = 82C37A operates with normal timing

Bit 4 = 0 = Channels have fixed priority, channel 0 having the highest priority and channel 3 the lowest priority

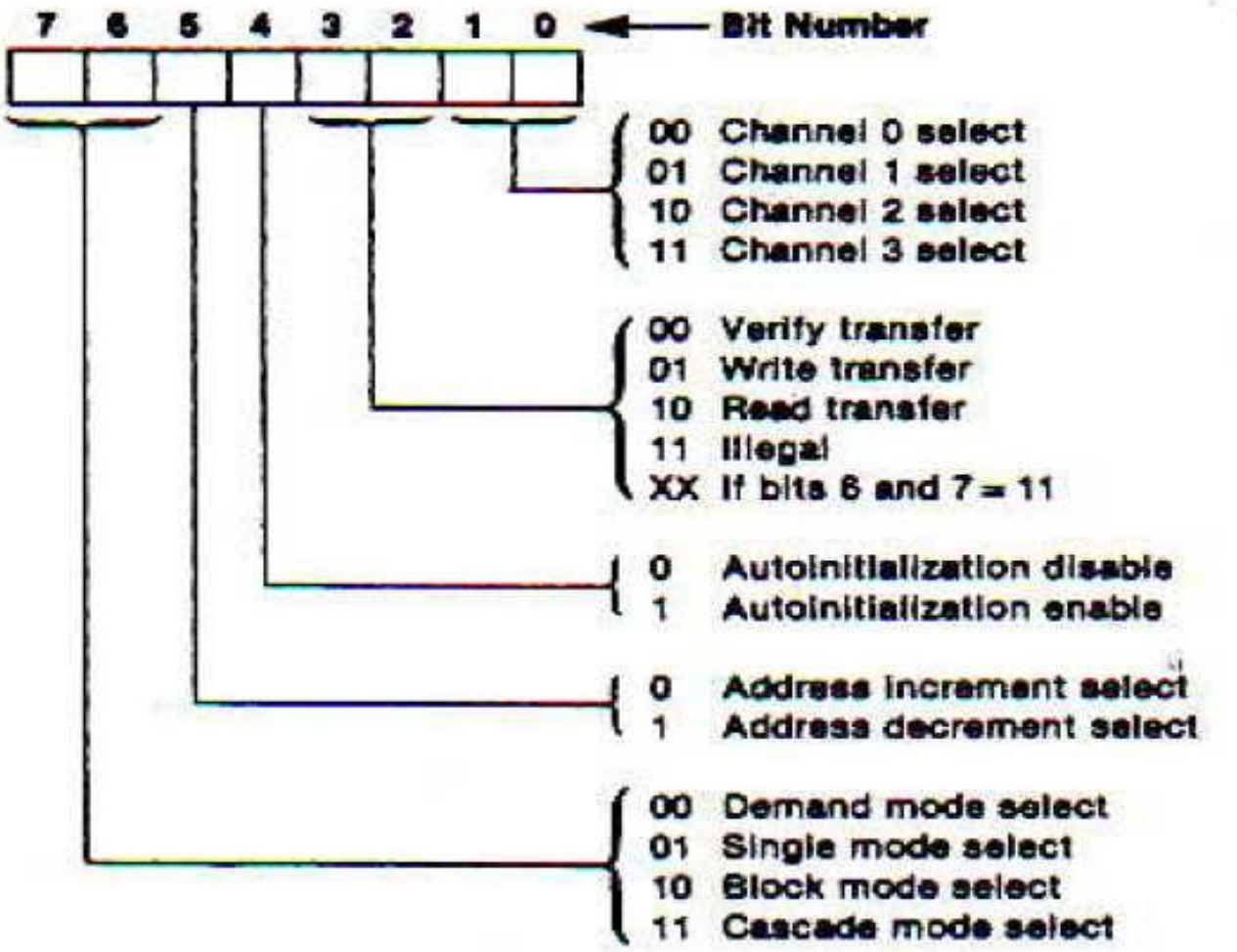
Bit 5 = 0 = Write operation occurs late in the DMA bus cycle

Bit 6 = 0 = DREQ is an active high (logic 1) signal

Bit 7 = 0 = DACK is an active low (logic 0) signal

Mode Registers

There is a separate mode register for each of the four DMA channels, each is eight bits in length. Their bits are used to select various operational features for the individual DMA channels.



Mode Registers

The two least significant bits are a 2-bit code, which identifies the channel to which the mode command byte applied.

The two most significant bits of the mode register select one of four possible modes of DMA operation for the channel:

Demand mode: bytes are continuously transferred as long as the DREQ signal remains active and the terminal count (TC) is not reached.

Single mode: used when it is necessary to not lock the microprocessor off the bus for the complete duration of the DMA operation.

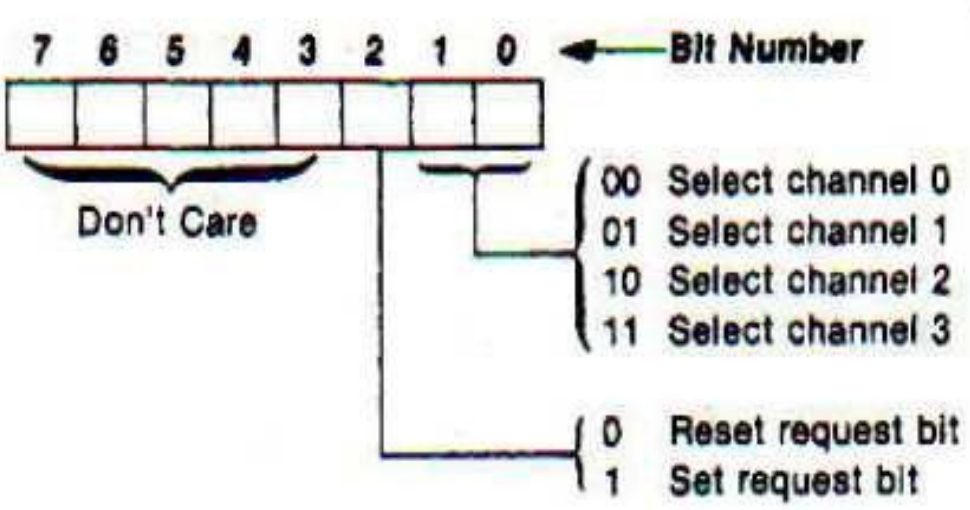
Block mode: DREQ can be released at any time after the DMA cycle begins, and the block transfer will still run to completion.

Cascade mode: used when more than one 8237 is present in a system.

Request Register

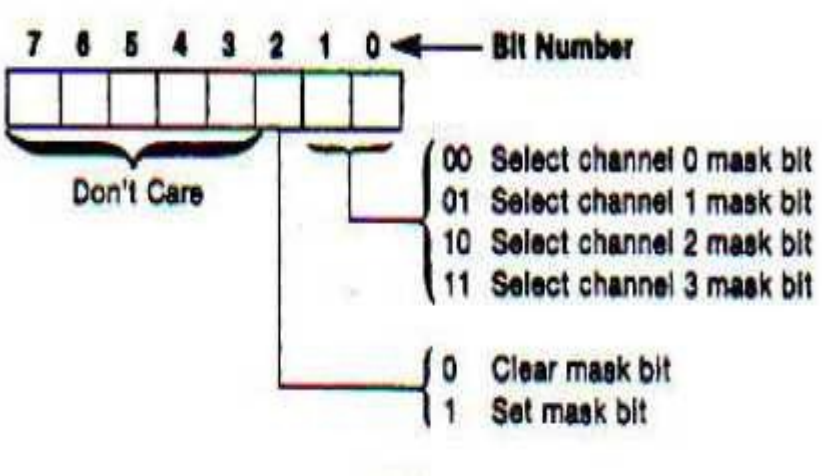
The **request register** is used to request a DMA transfer via software

When the request bit for a channel is set. DMA operation is started, and when reset. The DMA cycle is stopped. Any channel used for software-initiated DMA must be programmed for block-transfer mode of operation.

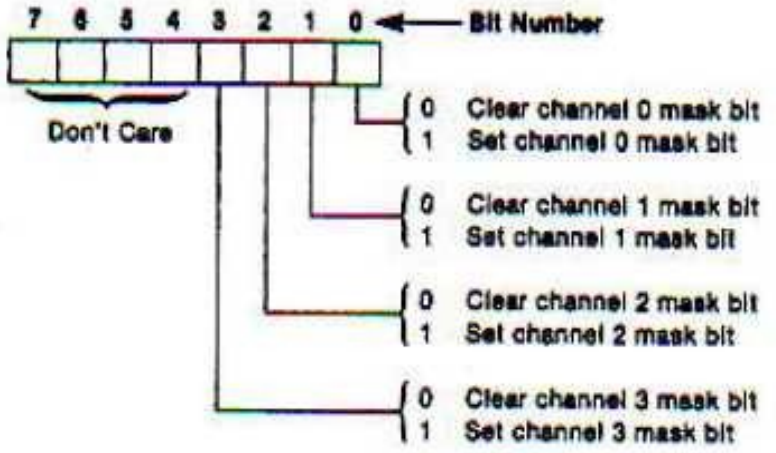


Mask Register

When a mask bit is set, the DREQ input for the corresponding channel is disabled. Therefore, hardware requests to the channel are ignored.



relative register address F_{16}

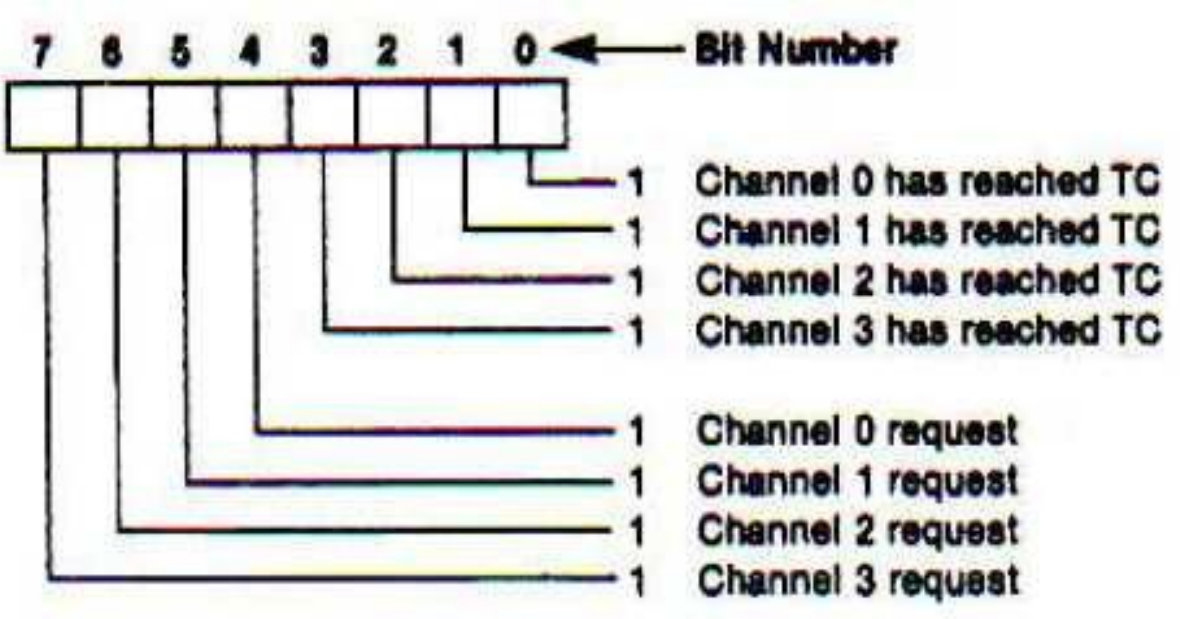


relative register address A_{16}.

At system initialization, it is a common practice to clear the mask register. Thus, we see that a special command is provided to perform this operation. Executing an output cycle to the register with relative address E_{16} clears the mask register.

Status Register

Contains information about the operating state of the four DMA channels.



The 8088 can read the contents of the status register through software. This is done by initiating an input bus cycle for register address 8_{16} relative to the base address for the 82C37A.

Temporary Register

during memory-to memory DMA transfers, the data read from the source address are held in a register known as the temporary register and then a write cycle is initiated to write the data to the destination address.

At the completion of the DMA cycle, this register contains the last byte that was transferred. The value in this register can be read by the microprocessor.

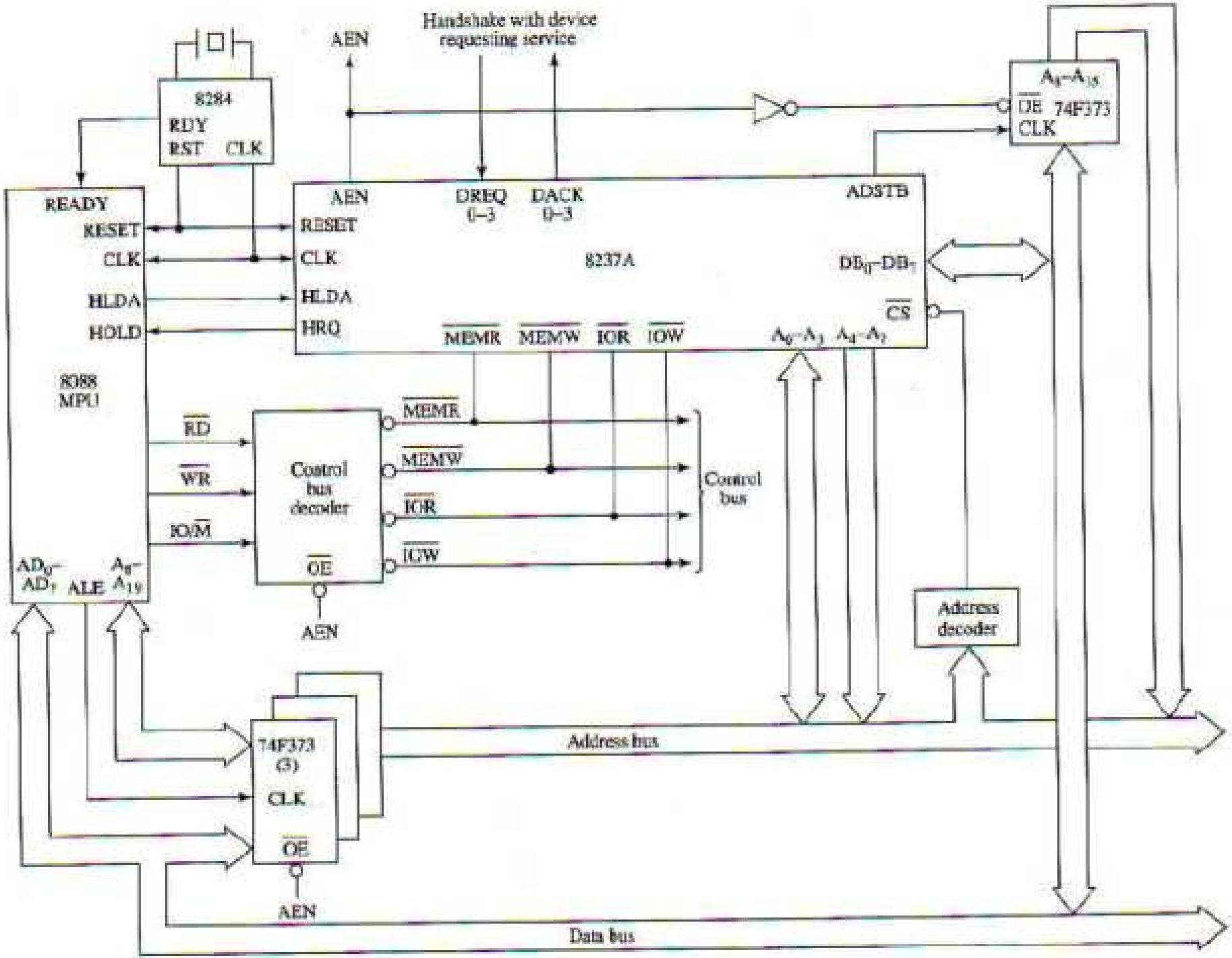
DMA Interface for the 8088-Based Microcomputer Using the 82C37A

Both the 8088 MPU and the 82C37A DMA controller drive the same three system buses: address bus, data bus. and control bus.

During the DMA operation, the 82C37A generates all of the bus signals that are needed to access I/O devices and the memory. It also generates the AEN signal, which is used to disable the microprocessor's connection to the system bus.

AEN does this by disabling the control bus decoder and the latches for the address bus. The microprocessor's connection to the data bus is also disabled in response to the hold request received on its HOLD input.

Remember that logic 1 at HOLD puts the data bus lines in the high-Z state, Thus, during a DMA operation, the 82C37A is in complete control of the address bus, control bus, and data bus.


Handshake with device requesting service
AEN
8284
RDY
RST
CLK
READY
RESET
CLK
HLDA
HOLD
8088
MPU
AD0–AD7
ALE
A8–A19
AEN
DREQ 0–3
DACK 0–3
RESET
CLK
HLDA
HRQ
8237A
ADSTB
DB0–DB7
CS
MEMR
MEMW
IOR
IOW
A0–A3
A4–A7
A8–A15
OE 74F373
CLK
RD
WR
IO/M
Control bus decoder
OE
AEN
Control bus
Address decoder
74F373 (3)
CLK
OE
AEN
Address bus
Data bus