SUBJECT:

ANALOG & DIGITAL ELECTRONICS

TOPIC: **RECTIFIERS**

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EEE

DEFINITION

Key Point : *A **rectifier** is a device which converts a.c. voltage to pulsating d.c. voltage, using one or more p-n junction diodes.*

The p-n junction diode conducts only in one direction. It conducts when forward biased while practically it does not conduct when reverse biased. Thus if an alternating voltage is applied across a p-n junction diode, during positive half cycle the diode will be forward biased and will conduct successfully. While during the negative half cycle it will be reversed biased and will not conduct at all. Thus the conduction occurs only during positive half cycle. If the resistance is connected in series with the diode, the output voltage across the resistance will be unidirectional i.e. d.c. Thus p-n junction diode subjected to an a.c. voltage acts as a rectifier converting alternating voltage to a pulsating d.c. voltage.

TYPES OF RECTIFIERS:

- HALF WAVE RECTIFIER
- FULLWAVE RECTIFIER
- BRIDGE RECTIFIER

HALF WAVE RECTIFIER

In half wave rectifier, rectifying element conducts only during positive half cycle of input a.c. supply. The negative half cycles of a.c. supply are eliminated from the output.

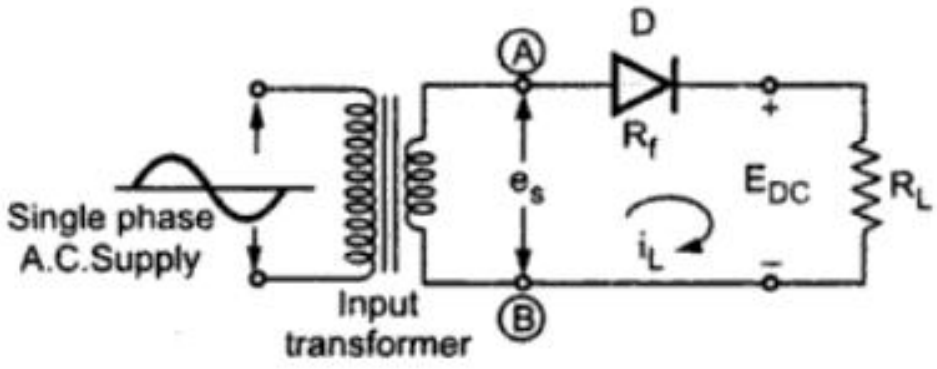


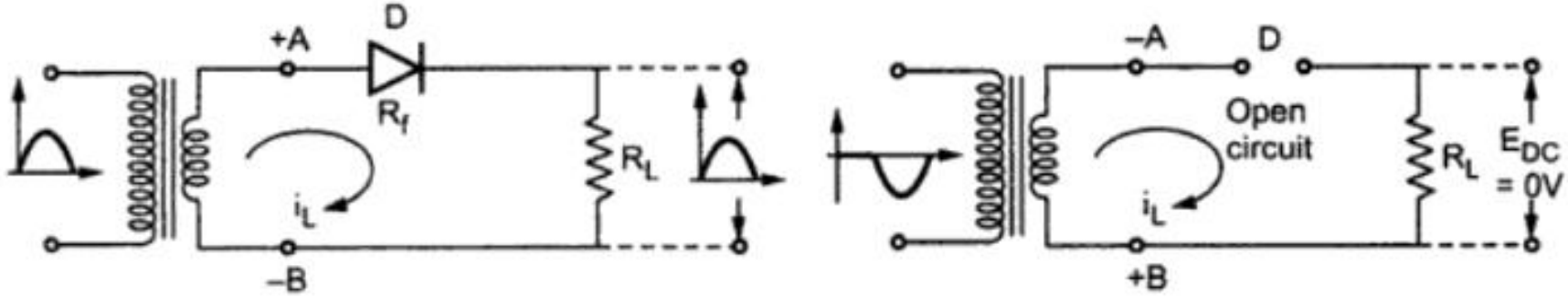
Fig. 3.3 Halfwave rectifier

This rectifier circuit consists of resistive load, rectifying element, i.e. p-n junction diode, and the source of a.c. voltage, all connected in series. The circuit diagram is shown in the Fig. 3.3. Usually, the rectifier circuits are operated from ac mains supply. To obtain the desired d.c. voltage across the load, the a.c. voltage is applied to rectifier circuit using suitable step-up or step-down transformer, mostly a step-down one, with necessary turns ratio.

OPERATION

During the positive half cycle of secondary a.c voltage, terminal (A) becomes positive with respect to terminal (B). The diode is forward biased and the current flows in the circuit in the clockwise direction, as shown in the Fig. 3.4 (a). The current will flow for almost full positive half cycle. This current is also flowing through load resistance R_L hence denoted as i_L, the load current.

During negative half cycle when terminal (A) is negative with respect to terminal (B), diode becomes reverse biased. Hence no current flows in the circuit as shown in the Fig. 3.4 (b). Thus the circuit current, which is also the load current, is in the form of half sinusoidal pulses.



(a) Diode forward biased **(b) Diode reverse biased**

Fig. 3.4

WAVEFORMS

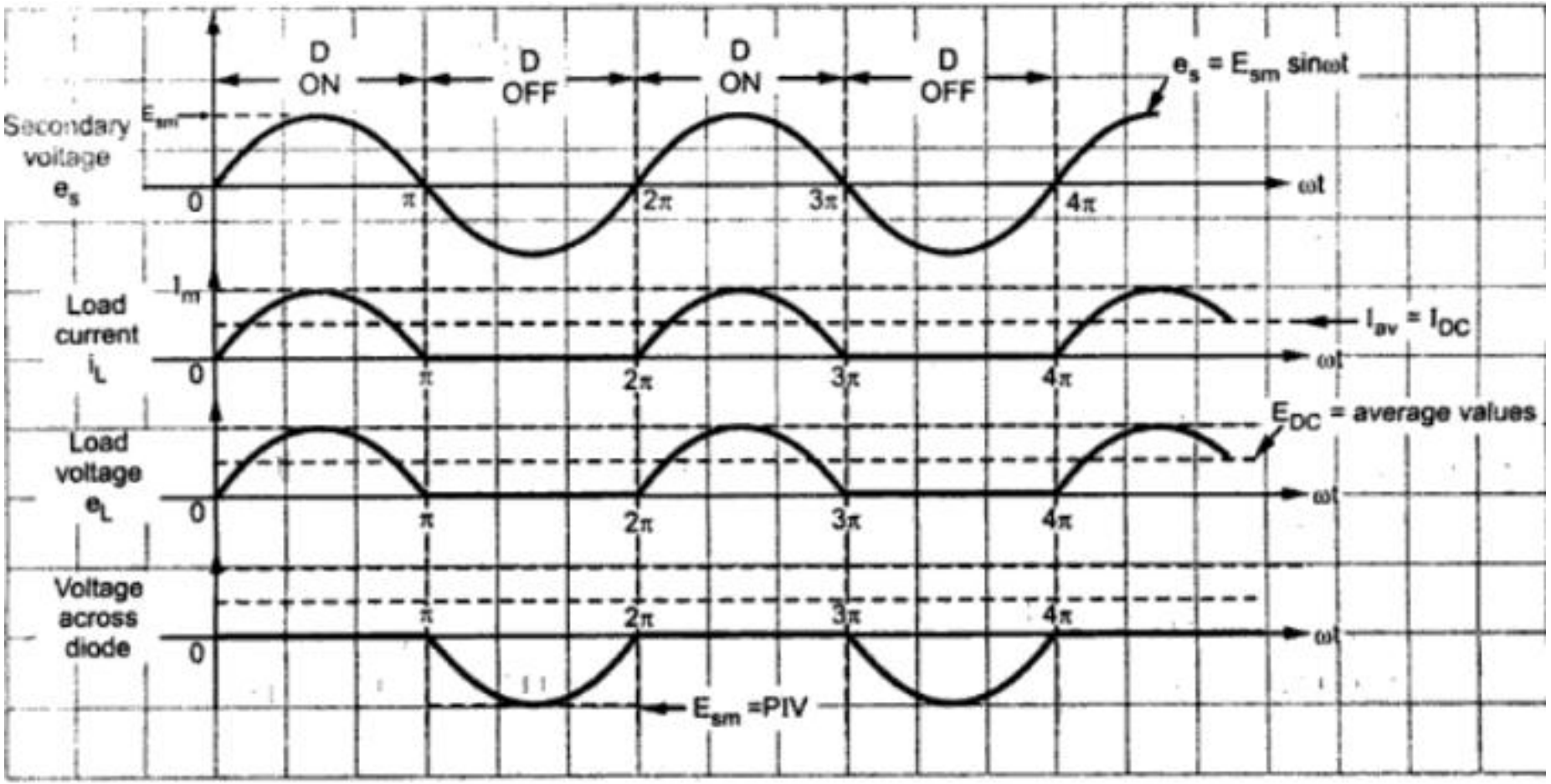


Fig. 3.5 Load current and load voltage waveforms for half wave rectifier

NEED OF CALCULATING AVERAGE:

Key Point: *Hence the output is called* ***pulsating d.c****. It is discontinuous in nature. Hence it is necessary to calculate the average value of load current and average value of output voltage.*

Average DC Load Current (I_{DC})

The average or dc value of alternating current is obtained by integration.

For finding out the average value of an alternating waveform, we have to determine the area under the curve over one complete cycle i.e. from 0 to 2π and then dividing it by the base i.e. 2π .

Mathematically, current waveform can be described as,

$$i_L = I_m \sin \omega t \qquad \text{for } 0 \le \omega t \le \pi$$

$$i_L = 0 \qquad \text{for } \pi \le \omega t \le 2\pi$$

where I_m = peak value of load current

$$\therefore \quad I_{DC} = \frac{1}{2\pi}\int_0^{2\pi} i_L \, d(\omega t) = \frac{1}{2\pi}\int_0^{2\pi} I_m \sin(\omega t)\, d(\omega t)$$

As no current flows during negative half cycle of a.c. input voltage, i.e. between $\omega t = \pi$ to $\omega t = 2\pi$, we change the limits of integration.

$$\therefore \quad I_{DC} = \frac{1}{2\pi}\int_0^{\pi} I_m \sin(\omega t)\, d(\omega t) = \frac{I_m}{2\pi}\left[-\cos(\omega t)\right]_0^{\pi}$$

$$= -\frac{I_m}{2\pi}\left[\cos(\pi) - \cos(0)\right] = -\frac{I_m}{2\pi}[-1-1] = \frac{I_m}{\pi}$$

$$\therefore \quad \boxed{I_{DC} = \frac{I_m}{\pi} = \text{average value}}$$

Applying Kirchhoff's voltage law we can write,

$$\boxed{I_m = \frac{E_{sm}}{R_f + R_L + R_s}}$$

where R_s = resistance of secondary winding of transformer. If R_s is not given it should be neglected while calculating I_m.

Average DC Load Voltage (E_{DC})

It is the product of average D.C. load current and the load resistance R_L.

$$E_{DC} = I_{DC}R_L$$

The winding resistance R_s and forward diode resistance R_f are practically very small compared to R_L.

$$\therefore \quad \boxed{E_{DC} = \frac{E_{sm}}{\pi\left[\frac{R_f + R_s}{R_L} + 1\right]}}$$

But as R_f and R_s are small compared to R_L, $(R_f + R_s)/R_L$ is negligibly small compared to 1. So neglecting it we get,

$$\therefore \quad \boxed{E_{DC} \approx \frac{E_{sm}}{\pi}}$$

3.3.4 R.M.S. Value of Load Current (I_{RMS})

The R.M.S means squaring, finding mean and then finding square root. Hence R.M.S. value of load current can be obtained as,

$$I_{RMS} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} (I_m \sin \omega t)^2 \, d(\omega t)} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} \left(I_m^2 \sin^2 \omega t \, d(\omega t)\right)}$$

$$= I_m \sqrt{\frac{1}{2\pi}\int_0^{\pi} \frac{[1-\cos(2\omega t)]\, d(\omega t)}{2}} = I_m \sqrt{\frac{1}{2\pi}\left\{\frac{\omega t}{2} - \frac{\sin(2\omega t)}{4}\right\}_0^{\pi}}$$

$$= I_m \sqrt{\frac{1}{2\pi}\left(\frac{\pi}{2}\right)} \qquad \text{as } \sin(2\pi) = \sin(0) = 0$$

$$= \frac{I_m}{2}$$

$$\therefore \quad \boxed{I_{RMS} = \frac{I_m}{2}}$$

3.3.8 Ripple Factor (γ)

It is seen that the output of half wave rectifier is not pure d.c. but a pulsating d.c. The output contain pulsating components called **ripples.** Ideally there should not be any ripples in the rectifier output. The measure of such ripples present in the output is with the help of a factor called **ripple factor** denoted by γ. It tells how smooth is the output. Smaller the ripple factor closer is the output to a pure d.c. The ripple factor expresses how much successful the circuit is in obtaining pure d.c. from a.c. input.

Mathematically ripple factor is defined as the ratio of R.M.S. value of the a.c. component to the average or d.c.component.

$$\text{Ripple factor} \quad \gamma = \frac{\text{R.M.S. value of a.c. component}}{\text{Average or d.c.component}}$$

Now the output current is composed of a.c. component as well as d.c. component.

Let I_{ac} = r.m.s. value of a. c. component present in output

I_{DC} = d.c. component present in output

I_{RMS} = R.M.S. value of total output current

$$\therefore \quad I_{RMS} = \sqrt{I_{ac}^2 + I_{DC}^2}$$

$$\therefore \quad I_{ac} = \sqrt{I_{RMS}^2 - I_{DC}^2}$$

Now Ripple factor $= \dfrac{I_{ac}}{I_{DC}}$ as per definition

$$\therefore \quad \gamma = \frac{\sqrt{I_{RMS}^2 - I_{DC}^2}}{I_{DC}}$$

$$\therefore \quad \gamma = \sqrt{\left(\frac{I_{RMS}}{I_{DC}}\right)^2 - 1}$$

This is the general expression for ripple factor and can be used for any rectifier circuit.

Now for a half wave circuit,

$$I_{RMS} = \frac{I_m}{2} \quad \text{while} \quad I_{DC} = \frac{I_m}{\pi}$$

$$\therefore \quad \gamma = \sqrt{\left[\frac{\left(\frac{I_m}{2}\right)}{\left(\frac{I_m}{\pi}\right)}\right]^2 - 1} = \sqrt{\frac{\pi^2}{4} - 1} = \sqrt{1.4674}$$

$$\therefore \quad \gamma = 1.211$$

3.3.13 Disadvantages of Half Wave Rectifier Circuit

The various disadvantages of the half wave rectifier circuit are,

1. The ripple factor of half wave rectifier circuit is 1.21, which is quite high. The output contains lot of varying components.
2. The maximum theoretical rectification efficiency is found to be 40%. The practical value will be less than this. This indicates that half wave rectifier circuit is quite inefficient.
3. The circuit has low transformer utilization factor, showing that the transformer is not fully utilized.
4. The d.c. current is flowing through the secondary winding of the transformer which may cause dc saturation of the core of the transformer. To minimize the saturation, transformer size have to be increased accordingly. This increases the cost.

FULL WAVE RECTIFIER

The full wave rectifier conducts during both positive and negative half cycles of input a.c. supply. In order to rectify both the half cycles of a.c. input, two diodes are used in this circuit. The diodes feed a common load R_L with the help of a center tap transformer. The a.c. voltage is applied through a suitable power transformer with proper turns ratio.

The full wave rectifier circuit is shown in the Fig. 1.53.

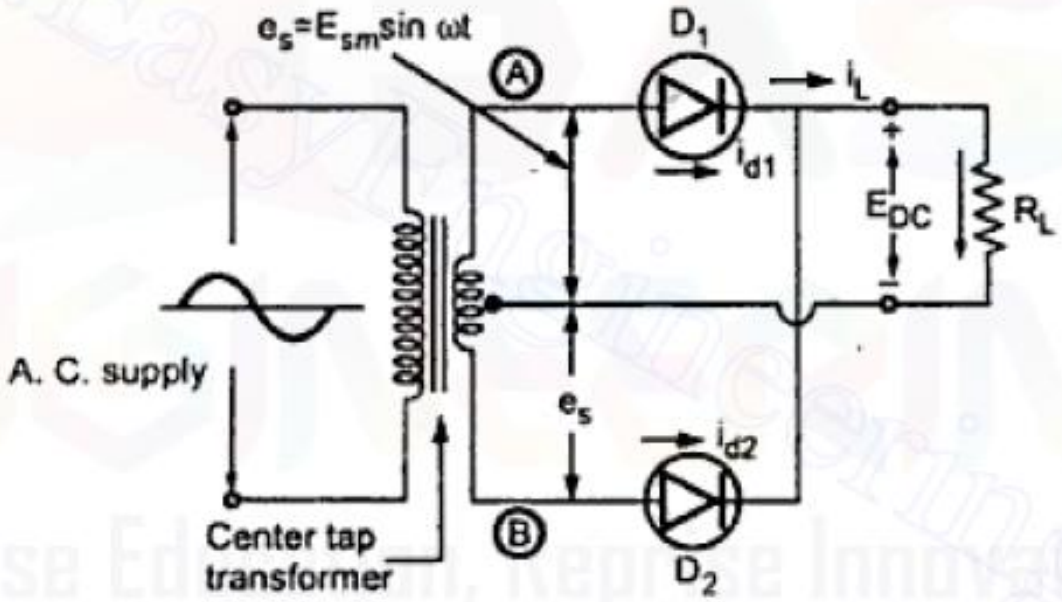


Fig. 1.53 Full wave rectifier

OPERATION

Consider the positive half cycle of a.c. input voltage in which terminal (A) is positive and terminal (B) negative. The diode D_1 will be forward biased and hence will conduct; while diode D_2 will be reverse biased and will act as an open circuit and will not conduct. This is illustrated in the Fig. 1.54.

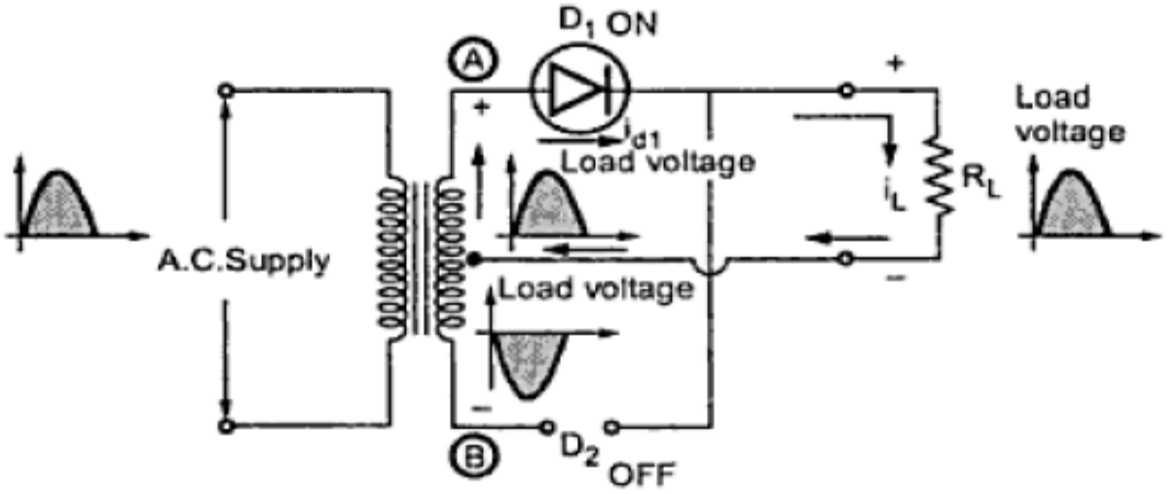


Fig. 1.54 Current flow during positive half cycle

The diode D_1 supplies the load current, i.e. $i_L = i_{d1}$. This current is flowing through upper half of secondary winding while the lower half of secondary winding of the transformer carries no current since diode D_2 is reverse biased and acts as an open circuit.

In the next half cycle of a.c. voltage, polarity reverses and terminal (A) becomes negative and (B) positive. The diode D_2 conducts, being forward biased, while D_1 does not, being reverse biased. This is shown in the Fig. 1.55.

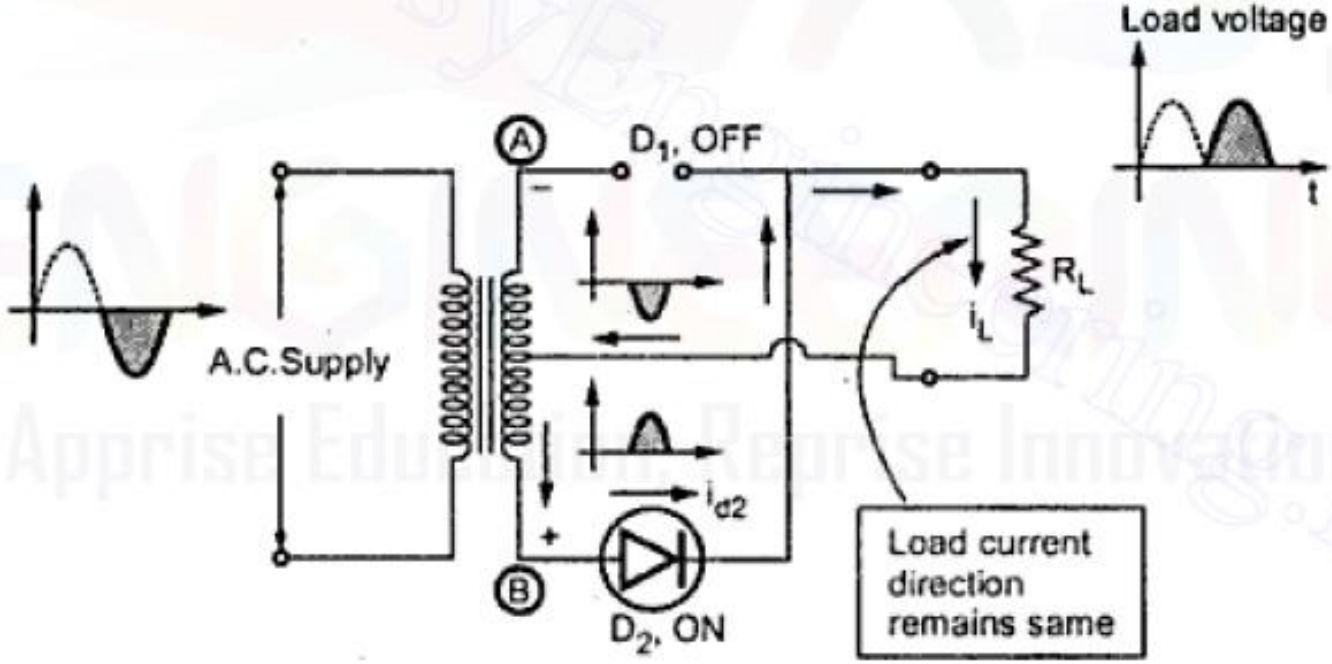


Fig. 1.55 Current flow during negative half cycle

The diode D_2 supplies the load current, i.e. $i_L = i_{d2}$. Now the lower half of the secondary winding carries the current but the upper half does not.

It is noted that the load current flows in both the half cycles of a.c. voltage and in the same direction through the load resistance. Hence we get rectified output across the load. The load current is sum of individual diode currents flowing in corresponding half cycles. It is also noted that the two diodes do not conduct simultaneously but in alternate half cycles.The individual diode currents and the load current are shown in the Fig. 1.56.

WAVEFORMS

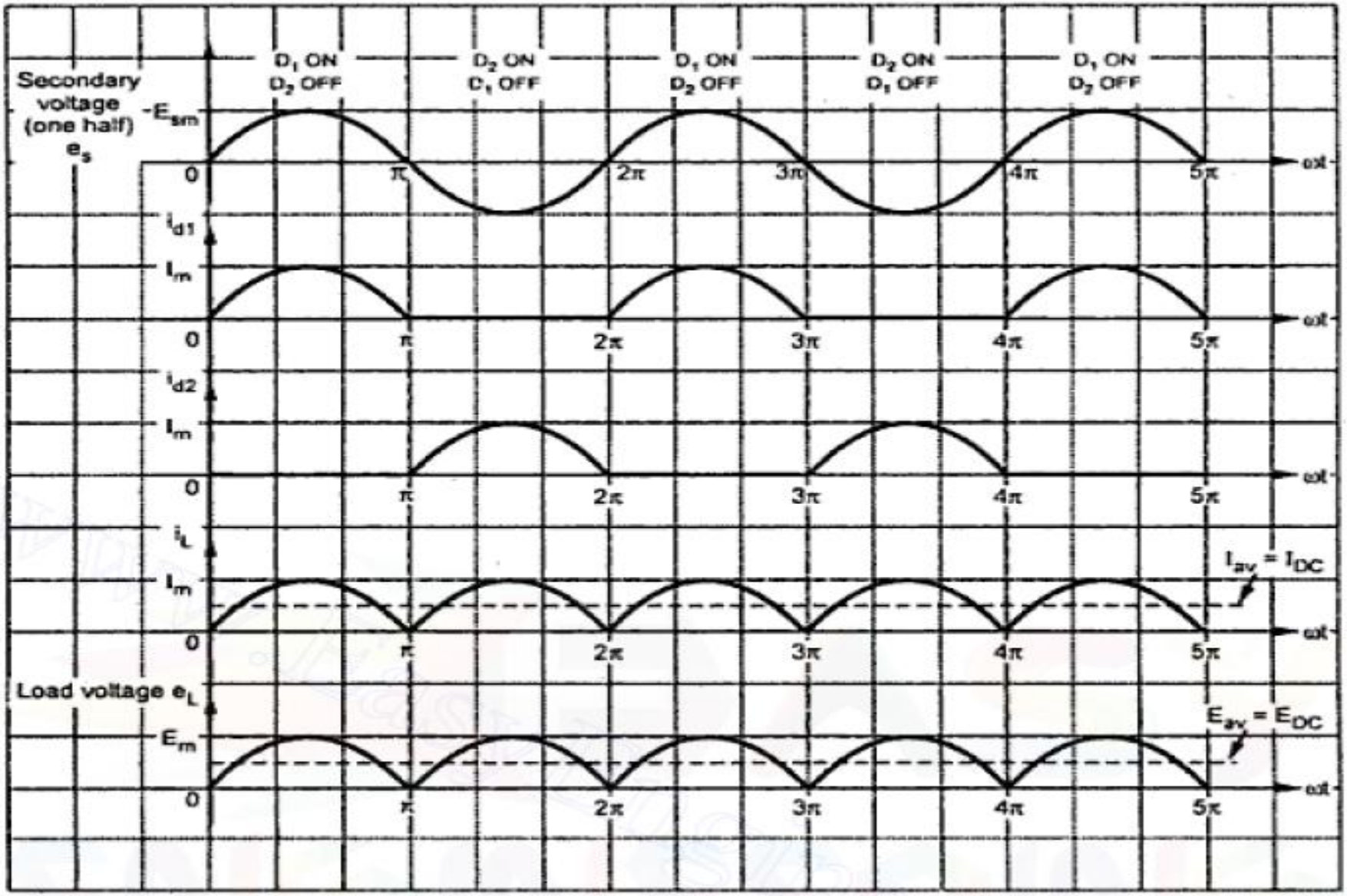


Fig. 1.56 Load current and voltage waveforms for full wave rectifier

1.26.3 Average D.C. Load Current (I_{DC})

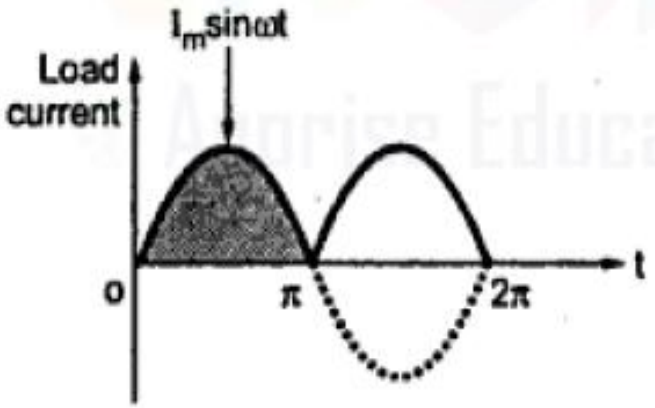


Fig. 1.58 Load current waveform

Consider one cycle of the load current i_L from 0 to π to obtain the average value which is d.c. value of load current.

$$i_L = I_m \sin \omega t \qquad 0 \leq \omega t \leq \pi$$

$$I_{av} = I_{DC} = \frac{1}{\pi}\int_0^{\pi} i_L \, d(\omega t) = \frac{1}{\pi}\int_0^{\pi} I_m \sin \omega t \, d(\omega t)$$

$$\therefore \quad = \frac{I_m}{\pi}\left[(-\cos \omega t)_0^{\pi}\right]$$

$$= \frac{I_m}{\pi}[-\cos \pi - (-\cos 0)] \qquad \ldots \cos \pi = -1$$

$$= \frac{I_m}{\pi}(+1 - (-1))]$$

$$\therefore \quad \boxed{I_{DC} = \frac{2I_m}{\pi}} \qquad \text{for full wave rectifier}$$

For half wave it is I_m/π and full wave rectifier is the combination of two half wave circuits acting alternately in two half cycles of input. Hence obviously the d.c. value for full wave circuit is $2\,I_m/\pi$.

1.26.4 Average D.C. Load Voltage (E_{DC})

The d.c. load voltage is,

$$E_{DC} = I_{DC}R_L = \frac{2I_m R_L}{\pi}$$

Substituting value of I_m,

$$E_{DC} = \frac{2E_{sm}R_L}{\pi[R_f + R_s + R_L]} = \frac{2E_{sm}}{\pi\left[1 + \frac{R_f + R_s}{R_L}\right]}$$

But as R_f and $R_s << R_L$ hence $\frac{R_f + R_s}{R_L} << 1$

$\therefore$

$$\boxed{E_{DC} = \frac{2E_{sm}}{\pi}}$$

1.26.5 RMS Load Current (I_{RMS})

The R.M.S. value of current can be obtained as follows :

$$I_{RMS} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_L^2 d(\omega t)}$$

Since two half wave rectifier are similar in operation we can write,

$$I_{RMS} = \sqrt{\frac{2}{2\pi}\int_0^{\pi} [I_m \sin \omega t]^2 d(\omega t)}$$

$$= I_m \sqrt{\frac{1}{\pi}\int_0^{\pi}\left[\frac{1-\cos 2\omega t}{2}\right] d(\omega t)} \qquad \text{as } \sin^2 \omega t = \frac{1-\cos 2\omega t}{2}$$

$$\therefore \quad I_{RMS} = I_m \sqrt{\frac{1}{2\pi}\left[[\omega t]_0^{\pi} - \left(\frac{\sin 2\omega t}{2}\right)_0^{\pi}\right]} = I_m \sqrt{\frac{1}{2\pi}[\pi - 0]}$$

$$= I_m \sqrt{\frac{1}{2\pi}(\pi)} \qquad \text{as } \sin(2\pi) = \sin(0) = 0$$

$$\therefore \quad \boxed{I_{RMS} = \frac{I_m}{\sqrt{2}}}$$

Ripple factor

3.4.9 Ripple Factor (γ)

As derived earlier in case of half wave rectifier the ripple factor is given by a general expression,

$$\text{Ripple factor} = \sqrt{\left[\frac{I_{RMS}}{I_{DC}}\right]^2 - 1}$$

For full wave $I_{RMS} = I_m/\sqrt{2}$ and $I_{DC} = 2I_m/\pi$ so,

substituting in the above equation.

$$\text{Ripple factor} = \sqrt{\left[\frac{I_m/\sqrt{2}}{2I_m/\pi}\right]^2 - 1}$$

$$= \sqrt{\frac{\pi^2}{8} - 1}$$

$$\therefore \quad \text{Ripple factor} = \gamma = 0.48$$

This indicates that the ripple contents in the output are 48 % of the d.c. component which is much less than that for half wave circuit.

ADVANTAGES & DISADVANTAGES OF FWR

1.26.15 Advantages of Full Wave Rectifier

1. The d.c. load voltage and current are more than half wave.
2. No d.c. current through transformer windings hence no possibility of saturation.
3. T.U.F. is better as transformer losses are less.
4. The efficiency is higher.
5. The large d.c. power output.
6. The ripple factor is less.

1.26.16 Disadvantages of Full Wave Rectifier

1. The PIV rating of diode is higher.
2. Higher PIV diodes are larger in size and costlier.
3. The cost of centre tap transformer is higher.

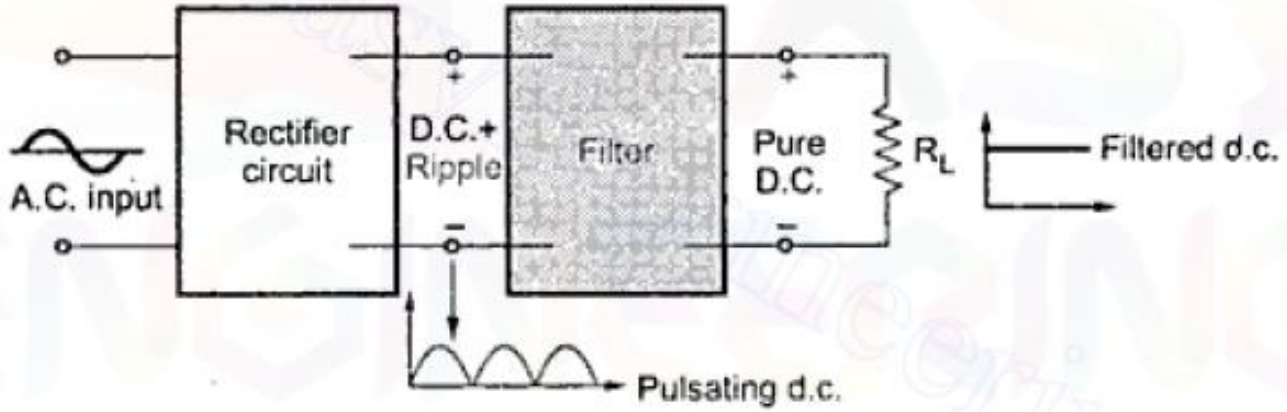
COMPARISION OF HWR & FWR

2. E_{DC}	$E_{DC} = \frac{E_{sm}}{\pi}$	$E_{DC} = \frac{2E_{sm}}{\pi}$, Higher
3. I_{DC}	$I_{DC} = \frac{I_m}{\pi}$	$I_{DC} = \frac{2I_m}{\pi}$, Higher
4. P_{DC}	$P_{DC} = \frac{I_m^2}{\pi^2} R_L$	$P_{DC} = \frac{4I_m^2}{\pi^2} R_L$, Four times higher
5. % η_{max}	40.6 %	81.2 %
6. Ripple factor	$\gamma = 1.211$	$\gamma = 0.48$, Ripple contents are less
7. Ripple frequency	f = 50 Hz	f = 100 Hz, Higher ripple frequency reduces the size of filter components, reducing the cost.
8. PIV	PIV = E_{sm}	PIV = 2 E_{sm}, Large rating diodes are. required.
9. Transformer	Normal is required	Center tap is required so cost is high.
10. T.U.F.	T.U.F. = 0.287	T.U.F. = 0.693, transformer gets more utilized.
11. Core saturation	Transformer core saturation possible	No d.c. current through transformer so core saturation not possible.

FILTER

1.29 Filter Circuits

It is seen that the output a half-wave or full wave rectifier circuit is not pure d.c.; but it contains fluctuations or ripple, which are undesired. To minimize the ripple content in the output, filter circuits are used. These circuits are connected between the rectifier and load, as shown in the Fig. 1.67.



TYPES OF FILTERS

There are basically two types of filter circuits,

- Capacitor input filter
- Choke input filter

Since ideally, inductance acts as short circuit for d.c., it cannot be placed in shunt arm across the load, otherwise the d.c. will be shorted.

Key Point : *Hence, in a filter circuit, the inductance is always connected in series with the load.*

The inductance used in filter circuits is also called "**choke**".

Similarly, since the capacitance is open for d.c., i.e. it blocks d.c.; hence it cannot be connected in series with the load.

Capacitor filter

The Fig. 3.20 shows a full -wave rectifier circuit, followed by a capacitor input filter. The filter uses a single capacitor connected in shunt arm i.e. in parallel with the load resistance R_L.

In order to minimize the ripple in the output, the capacitor C used in the filter circuit is quite large, of the order of tens of microfarads.

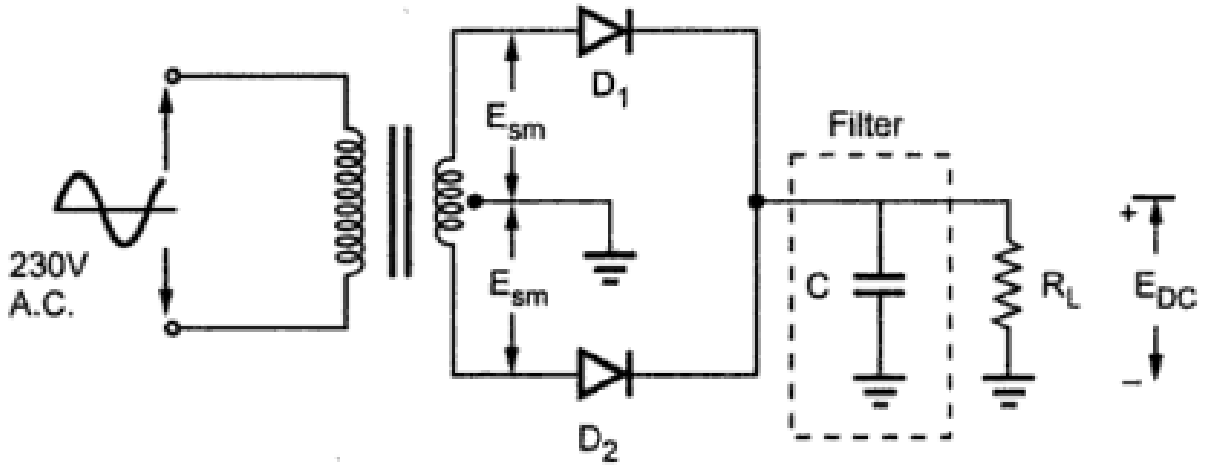


Fig. 3.20 Capacitor input filter

operation

During the first quarter cycle of the rectified output voltage, obtained from the rectifier circuit, the capacitor C gets charged to peak value E_{sm}. This is shown in the Fig.3.21.

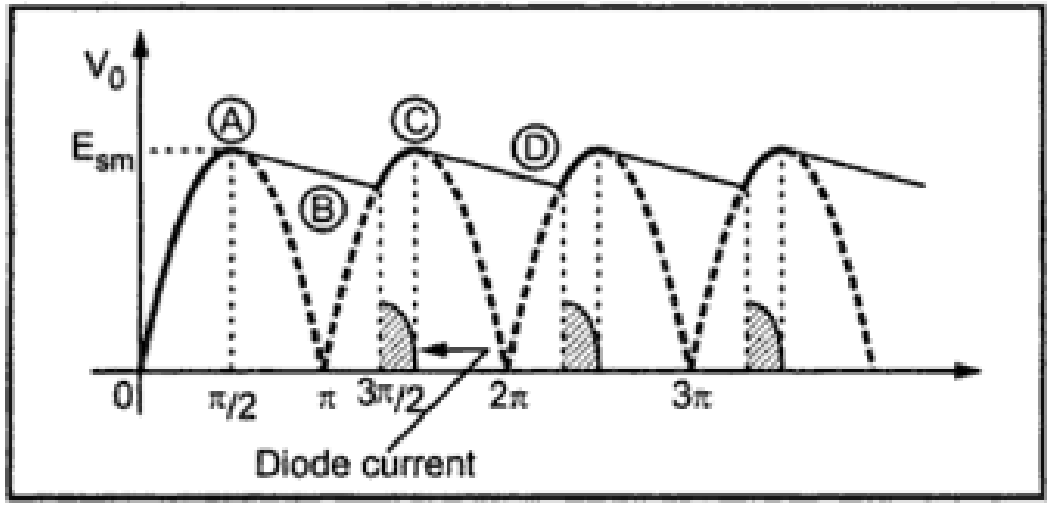


Fig. 3.21

Now in the next quarter cycle from $\frac{\pi}{2}$ to π, the rectifier output voltage, shown dotted starts decreasing. But as capacitor C is charged upto the maximum value E_{sm}, it makes the conducting diode reverse biased and the diode stops conducting. The current through diode reduces to zero when capacitor charges upto E_{sm} which is shown by a shaded portion in the Fig. 3.21.

Now the capacitor C starts discharging through load resistance R_L. As the capacitor C is large, the time constant CR_L is large and capacitor discharges to less extent, from point A to B as shown in Fig. 3.21. At this point, it can be seen that the rectifier output voltage, in the quarter π to $\frac{3\pi}{2}$ exceeds the capacitor voltage, at point B. And the another diode gets forward biased and starts conducting. The capacitor C, again starts charging and quickly gets charged through the forward biased diode having very small forward resistance. The time required by the capacitor to charge to the peak value is quite small and diode current again reduces to zero.

Expression of Ripple Factor for Capacitor Input Filter

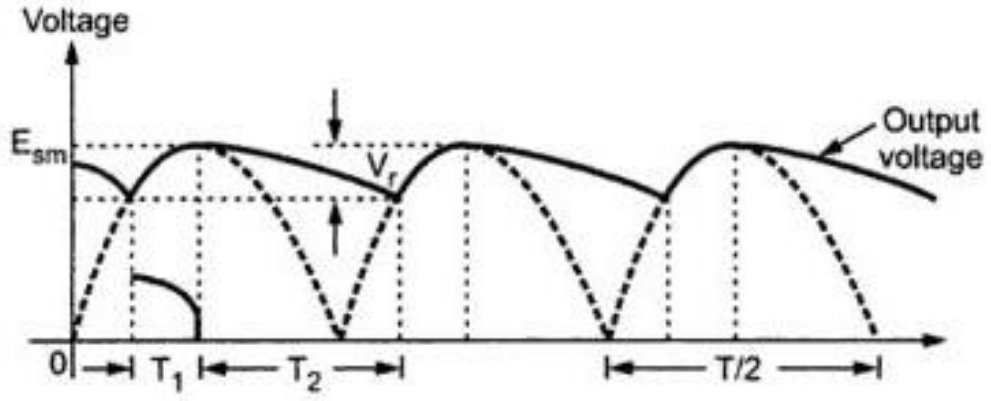


Fig. 3.25 (b)

Let $\frac{T}{2}$ be the time for half cycle of a.c. input voltage.

During the time interval T_1 the diode is conducting and the capacitor C is getting charged.

While in the time interval T_2 , the diode is reverse biased and the capacitor discharges through the load resistance R_L .

Let V_r be the peak to peak value of ripple voltage, which is assumed to be triangular as shown in the Fig. 3.26.

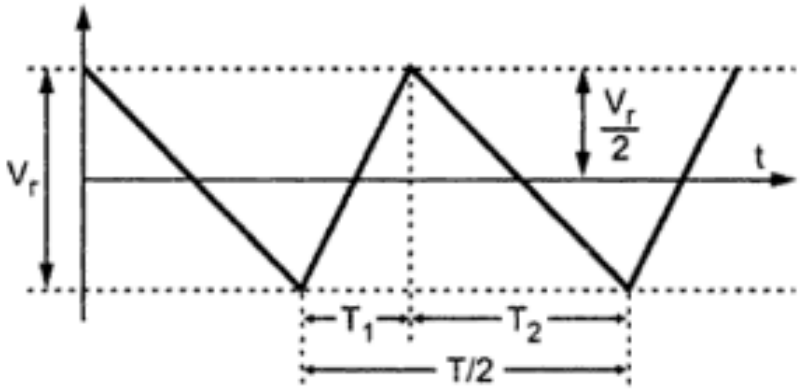


Fig. 3.26 Triangular approximation of ripple voltage

It can be shown mathematically that the r.m.s. value of such a triangular waveform is

$$V_{rms} = \frac{V_r}{2\sqrt{3}} \qquad \ldots (3.12)$$

During the time interval T_2, the capacitor C is discharging through the load resistance R_L. The charge lost is,

$$Q = CV_r \qquad \ldots (3.13)$$

But $$i = \frac{dQ}{dt}$$

$\therefore$ $$Q = \int_0^{T_2} i\,dt = I_{DC}\,T_2$$

As integration gives average or dc value

Hence $I_{DC}\, T_2 = CV_r$ ... (3.14)

$$\therefore \quad V_r = \frac{I_{DC}\, T_2}{C}$$

Now, $T_1 + T_2 = \frac{T}{2}$ Normally, $T_2 >> T_1$

$$\therefore \quad T_1 + T_2 \approx T_2 = \frac{T}{2} \quad \text{where } T = \frac{1}{f}$$

$$\therefore \quad V_r = \frac{I_{DC}}{C}\left[\frac{T}{2}\right] = \frac{I_{DC} \times T}{2C} = \frac{I_{DC}}{2\,fC}$$

But $I_{DC} = \frac{E_{DC}}{R_L}$

$$\therefore \quad V_r = \frac{E_{DC}}{2\,f\,C\,R_L} \qquad \text{... (3.15)}$$

$$\text{Ripple factor} = \frac{V_{rms}}{E_{DC}} = \frac{\frac{E_{DC}}{2fCR_L}}{2\sqrt{3}} \times \frac{1}{E_{DC}}, \text{ Since } V_{rms} = \frac{V_r}{2\sqrt{3}}$$

$$\therefore \quad \text{Ripple factor} = \frac{1}{4\sqrt{3}\, f C R_L} \text{ for full wave} \qquad \ldots (3.16)$$

For **half wave rectifier** with capacitor input filter the ripple factor is

$$\text{Ripple factor} = \frac{1}{2\sqrt{3}\, f C R_L} \text{ for half wave} \qquad \ldots (3.17)$$

The product CR_L is the time constant of the filter circuit.

Ex. 3.9 : *A 100 μF capacitor, when used as filtering element, has 12 V, d.c. across it with a terminal load resistance of 2 k Ω . If the rectifier is full-wave and supply frequency is 50 Hz, what is the percentage of ripple in the output ? Draw the neat circuit diagram.*

Sol. : The circuit diagram is shown in the Fig. 3.28.

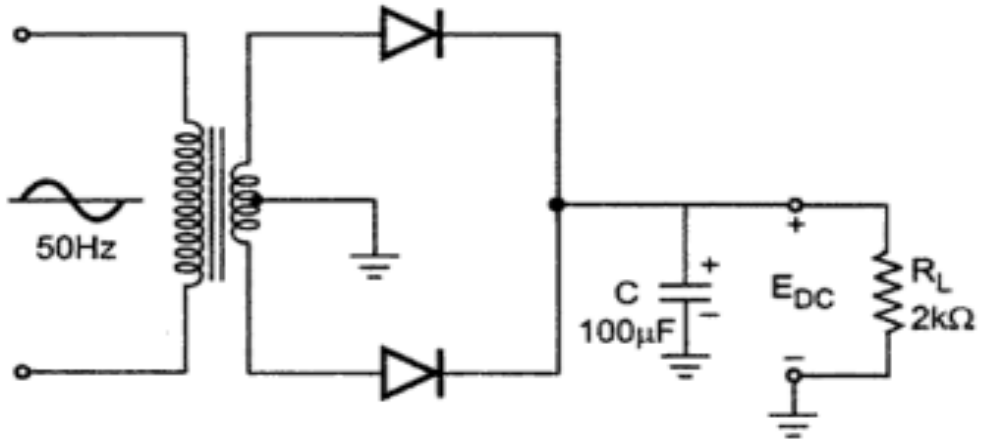


Fig. 3.28

Given : $R_L = 2k\,\Omega$, $C = 100\,\mu F$, $E_{DC} = 12$ V, Supply frequency = 50 Hz

$$\text{Ripple factor} = \frac{1}{4\sqrt{3}\, f C R_L} = \frac{1}{4\sqrt{3}\,[50][100\times10^{-6}\,][2\times10^{3}\,]}$$

$$= \frac{1}{4\sqrt{3}\,(50)\,(2\times10^{-1}\,)} = 0.01443$$

$\therefore$ % of ripple in the output $= 0.01443 \times 100 = 1.443\ \%$

Inductor filter

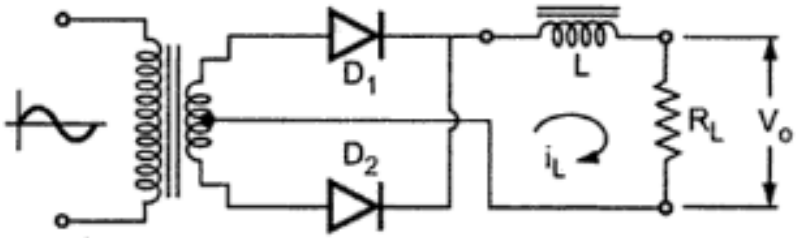


Fig. 3.31 (a) Circuit diagram of choke filter

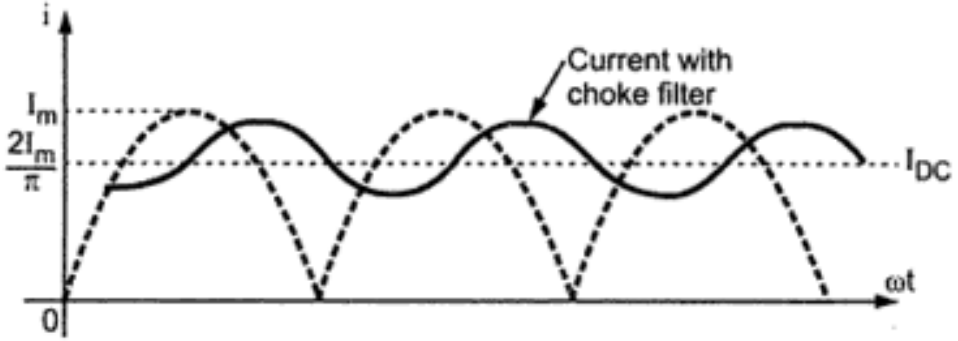


Fig. 3.31 (b) Current waveform of choke filter

operation

In the positive half cycle of the secondary voltage of the transformer, the diode D_1 is forward biased. Hence the current flows through D_1, L and R_L. While in the negative half cycle, the diode D_1 is reverse biased while diode D_2 is forward biased. Hence the current flows through D_2, L and R_L. Hence we get unidirectional current through R_L. Due to inductor L which opposes change in current, it tries to make the output smooth by opposing the ripple content in the output.

We know that the fourier series for the load current for full wave rectifier as,

$$i_L = I_m \left[\frac{2}{\pi} - \frac{4}{3\pi} \cos 2\omega t - \frac{4}{15\pi} \cos 4\omega t \right]$$

Neglecting higher order harmonics we get,

$$i_L = \frac{2I_m}{\pi} - \frac{4I_m}{3\pi} \cos 2\omega t \qquad \ldots (3.20)$$

Neglecting diode forward resistances and the resistance of choke and transformer secondary we can write the d.c. component of current as

$$\frac{2I_m}{\pi} = \frac{2V_m}{\pi R_L} \quad \text{... (3.21)}$$

as $$I_m = \frac{V_m}{R_L}$$

While the second harmonic component represents a.c. component or ripple present and can be written as,

$$I_m = \frac{V_m}{Z} \text{ for a.c. component} \quad \text{... (3.22)}$$

Now $$Z = R_L + j2X_L = \sqrt{R_L^2 + 4\omega^2 L^2} \angle \phi \quad \text{... (3.23)}$$

where $$\phi = \tan^{-1} \frac{2\omega L}{R_L} \quad \text{... (3.24)}$$

$$\therefore \quad I_m = \frac{V_m}{\sqrt{R_L^2 + 4\omega^2 L^2}} \quad \text{... (3.25)}$$

3.9.2 Expression for the Ripple Factor

Ripple factor is given by ,

$$\text{Ripple factor} = \frac{I_{rms}}{I_{DC}} \qquad \ldots (3.27)$$

where $I_{rms} = \frac{I_m}{\sqrt{2}}$ of a.c. component

$$I_{rms} = \frac{4\,V_m}{3\sqrt{2}\,\pi\sqrt{R_L^2 + 4\,\omega^2\,L^2}} \qquad \ldots (3.28)$$

while $$I_{DC} = \frac{2\,V_m}{\pi\,R_L} \qquad \ldots (3.29)$$

$$\therefore \quad \text{Ripple factor} = \frac{\dfrac{4\,V_m}{3\sqrt{2}\,\pi\sqrt{R_L^2 + 4\,\omega^2\,L^2}}}{\dfrac{2\,V_m}{\pi\,R_L}} \qquad \ldots (3.30)$$

$$= \frac{2}{3\sqrt{2}} \cdot \frac{1}{\sqrt{1 + \dfrac{4\,\omega^2\,L^2}{R_L^2}}} \qquad \ldots (3.31)$$

Initially on no load condition, $R_L \to \infty$ and hence $\frac{4\omega^2 L^2}{R_L^2} \to 0$.

$$\therefore \quad \text{Ripple factor} = \frac{2}{3\sqrt{2}} = 0.472 \qquad \ldots (3.32)$$

This is very close to normal full wave rectifier without filtering.

But as load increases, R_L decreases hence $\frac{4\omega^2 L^2}{R_L^2} >> 1$. So neglecting 1 we get,

$$\text{Ripple factor} = \frac{2}{3\sqrt{2}} \cdot \frac{1}{\sqrt{\frac{4\omega^2 L^2}{R_L^2}}} \qquad \ldots (3.33)$$

$$= \frac{R_L}{3\sqrt{2}.\omega L} \qquad \ldots (3.34)$$

So as load changes, ripple charges which is inversely proportional to the value of the inductor. Smaller the value of R_L, smaller is the ripple hence the filter is suitable for low load resistances i.e. for high load current applications.

3.10 L-Section Filter

This is also called **choke input filter** as the filter element looking from the rectifier side is an inductance L. The d.c. winding resistance of the choke is R_x . The circuit is also called L-type filter or LC filter. The circuit is shown in the Fig. 3.32.

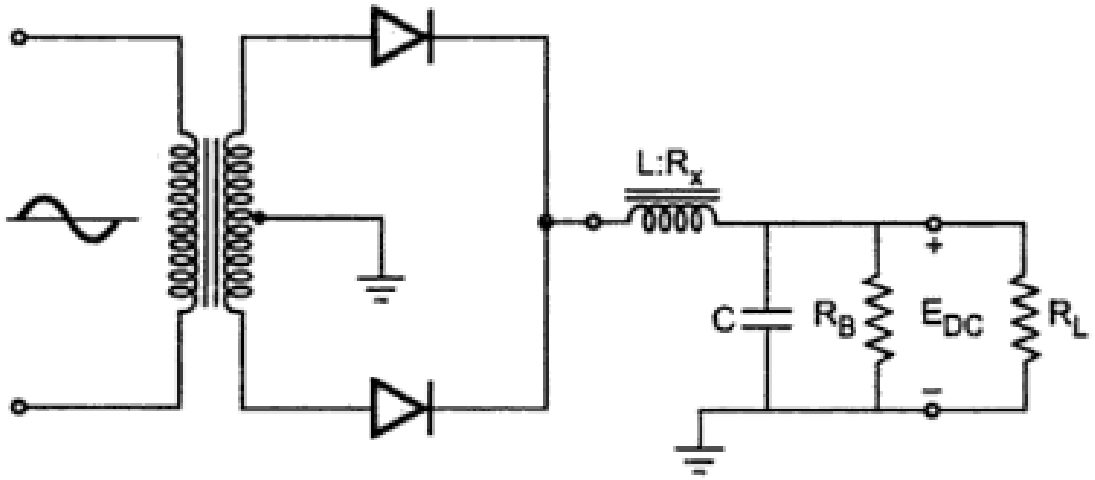


Fig. 3.32 Choke input filter

The basic requirement of this filter circuit is that the current through the choke must be continuous and not interrupted. An interrupted current through the choke may develop a large back e.m.f. which may be in excess of PIV rating of the diodes and /or maximum voltage rating of the capacitor C. Thus this back e.m.f. is harmful to the diodes and capacitor. To eliminate the back e.m.f. developed across the choke, the current through it must be maintained continuous.

Ripple factor

The d.c. current in the circuit will be,

$$I_{DC} = \frac{\frac{2}{\pi} E_{sm}}{R_x + R} \quad \text{... (3.39)}$$

$$R = R_B \,||\, R_L$$

$$\therefore \quad E_{DC} \text{ across the load} = I_{DC}\, R = \frac{2}{\pi} \frac{E_{sm}}{R_x + R} \times R$$

$$\therefore \quad E_{DC} = \frac{2}{\pi} \frac{E_{sm}}{1 + \frac{R_x}{R}} \quad \text{... (3.40)}$$

Normally, R_x is much less than R, i.e. $R_x << R$

Then, $$E_{DC} \approx \frac{2}{\pi} E_{sm} \quad \text{... (3.41)}$$

Thus the choke input filter circuit gives approximately constant d.c. voltage across the load. In other words, this filter circuit is having better load regulation compared to that of capacitor input filter in which case the d.c. load voltage depends upon the d.c. load current drawn. Let us calculate the ripple factor for choke input filter, based on the assumptions already made.

The impedance Z_2 of the filter circuit for second harmonic component of input, i.e. at 2ω, will be,

$$Z_2 = (R_x) + (j\, 2\omega L) + \left[\frac{1}{j2\,\omega C} \,||\, R \right] \quad \text{... (3.42)}$$

But, $\frac{1}{2\omega C} << R$, and $2\omega L >> R_x$, as per assumptions.

Hence, $$|Z_2| \approx 2\omega L \quad \text{... (3.43)}$$

Second harmonic component of the current in the filter circuit, will be

$$I_{2m} = \frac{\frac{4}{3\pi} E_{sm}}{Z_2} \approx \frac{\frac{4}{3\pi} E_{sm}}{2\omega L} \quad \text{... (3.44)}$$

The second harmonic voltage across the load is

$$E_{2m} = I_{2m} \times \left[\frac{1}{2\omega C} || R \right] \approx I_{2m} \times \frac{1}{2\omega C} \quad \text{... (3.45)}$$

Since, $$\frac{1}{2\omega C} << R$$

$$\therefore \quad E_{2m} = I_{2m} \times \frac{1}{2\omega C} = \frac{\frac{4}{3\pi} E_{sm}}{2\omega L} \times \frac{1}{2\omega C} \quad \text{... (3.46)}$$

$$\therefore \quad E_{2m} = \frac{4}{3\pi} \frac{E_{sm}}{4\omega^2 LC} = \frac{E_{sm}}{3\pi\omega^2 LC} \quad \text{... (3.47)}$$

$$\therefore \quad E_{2rms} = \frac{E_{2m}}{\sqrt{2}} = \frac{E_{sm}}{3\sqrt{2}\,\pi\,\omega^2 LC} \quad \text{... (3.48)}$$

Hence the ripple factor is given by,

$$\text{Ripple factor} = \frac{E_{2rms}}{E_{DC}} \qquad \ldots (3.49)$$

$$= \frac{E_{sm}}{3\sqrt{2}\,\pi\,\omega^2\,LC} \times \frac{1}{\frac{2}{\pi}\,\frac{E_{sm}}{1+\frac{R_x}{R}}}$$

$$= \frac{1}{6\omega^2\,LC\sqrt{2}}\left(1+\frac{R_x}{R}\right) \qquad \text{but } R_x << R$$

$$\therefore \quad \text{Ripple factor} \approx \frac{1}{6\sqrt{2}\,\omega^2\,LC} \qquad \ldots (3.50)$$

3.12 CLC Filter or π Filter

This is a capacitor filter followed by a L section filter. The ripple rejection capability of π filter is very good. It is shown in the Fig. 3.36.

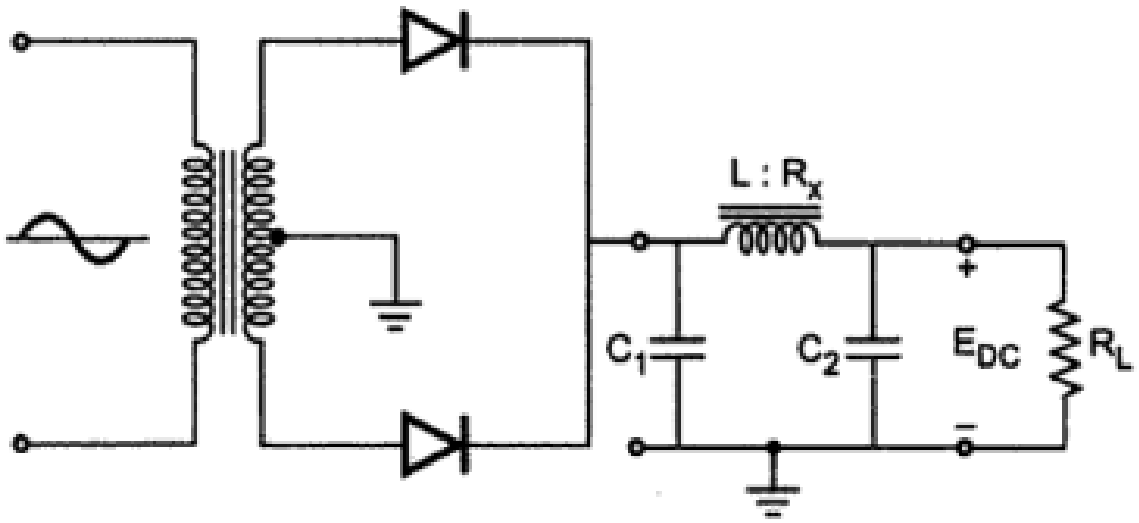


Fig. 3.36 π type filter

The rectifier output is given to the capacitor C_1. This capacitor offers very low reactance to the a.c. component but blocks d.c. component. Hence capacitor C_1 bypasses most of the a.c. component. The d.c. component then reaches to the choke L. The choke L offers very high reactance to a.c. component and low reactance to d.c. So it blocks a.c. component and does not allow it to reach to load while it allows d.c. component to pass through it. The capacitor C_2 now allows to pass remaining a.c. component and almost pure d.c. component reaches to the load. The circuit looks like a π hence called π filter. To obtain almost pure d.c. to the load, more such π sections may be used one after another.

The output voltage is given by,

$$E_{DC} = E_{sm} - \frac{V_r}{2} - I_{DC} R_x$$

where V_r = Peak to peak ripple voltage

3.12.1 Ripple Factor

The ripple factor for this filter is given by ,

$$\text{Ripple factor} = \frac{\sqrt{2} \times X_{C_1} \times X_{C_2}}{X_L \; R_L}$$

The various reactances X_{C_1}, X_{C_2}, X_L are to be calculated at twice the supply frequency since the circuit is fed from a full wave rectifier circuit.

Hence,

$$X_{C_1} = \frac{1}{2\omega C_1}$$

$$X_{C_2} = \frac{1}{2\omega C_2}$$

$$X_L = 2\omega L$$

$$\therefore \quad \text{Ripple factor} = \frac{\sqrt{2}\left(\frac{1}{2\omega C_1}\right)\left(\frac{1}{2\omega C_2}\right)}{(2\omega L)(R_L)}$$

$$\therefore \quad \gamma = \frac{\sqrt{2}}{8\omega^3 LC_1 C_2 R_L}$$

Since this π type filter employes three fitering elements, the riple is reduced to the great extent.

If C_1 and C_2 are expressed in microfarads and frequency f is assumed to be 50 Hz then we get,

$$\gamma = \frac{\sqrt{2}}{8(2\pi \times 50)^3 \times \left(C_1 \times 10^{-6} \times C_2 \times 10^{-6} \times L \times R_L\right)}$$

$$\therefore \quad \gamma \approx \frac{5700}{L C_1 C_2 R_L}$$

where C_1 and C_2 are in μF, L in henries and R_L in ohms.

Comparison

Table Comparison of Various Types of Filters

	Type of Filter				
	None	*L*	*C*	*L-Section*	*π-Section*
V_{dc} at no load	$0.636\,V_m$	$0.636\,V_m$	V_m	V_m	V_m
V_{dc} at load I_{dc}	$0.636\,V_m$	$0.636\,V_m$	$V_m - \frac{4170\,I_{dc}}{C}$	$0.636\,V_m$	$V_m - \frac{4170\,I_{dc}}{C}$
Ripple factor Γ	0.48	$\frac{R_L}{16000\,L}$	$\frac{2410}{CR_L}$	$\frac{0.83}{LC}$	$\frac{3330}{LC_1C_2R_L}$
Peak inverse voltage (PIV)	$2V_m$	$2V_m$	$2V_m$	$2V_m$	$2V_m$

BIPOLAR JUNCTION TRANSISTOR

BY

K.SUDHEER

Before transistor, the amlification was achieved by using vaccum tubes as an amplifier. Now-a-days vaccum tubes are replaced by transistors because of following advantages of transistors.

- Low operating voltage
- Higher efficiency
- Small size and ruggedness and
- Does not require any filament power

Transistor types

When a transistor is formed by sandwiching a single p–region between two n-regions, as shown in the Fig. 4.1 (a), it is an n-p-n type transistor. The p-n-p type transistor has a single n-region between two p-regions, as shown in Fig. 4.1(b).

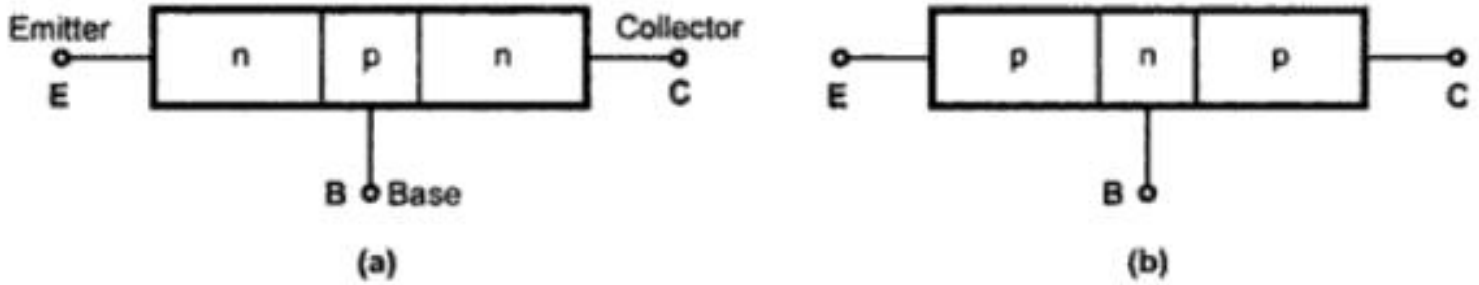


Fig. 4.1 Bipolar transistor construction

The middle region of each transistor type is called the base of the transistor. This region is very thin and lightly doped. The remaining two regions are called **emitter** and **collector**. The emitter and collector are heavily doped. But the doping level in emitter is slightly greater than that of collector and the collector region-area is slightly more than that of emitter.

Transistor symbols

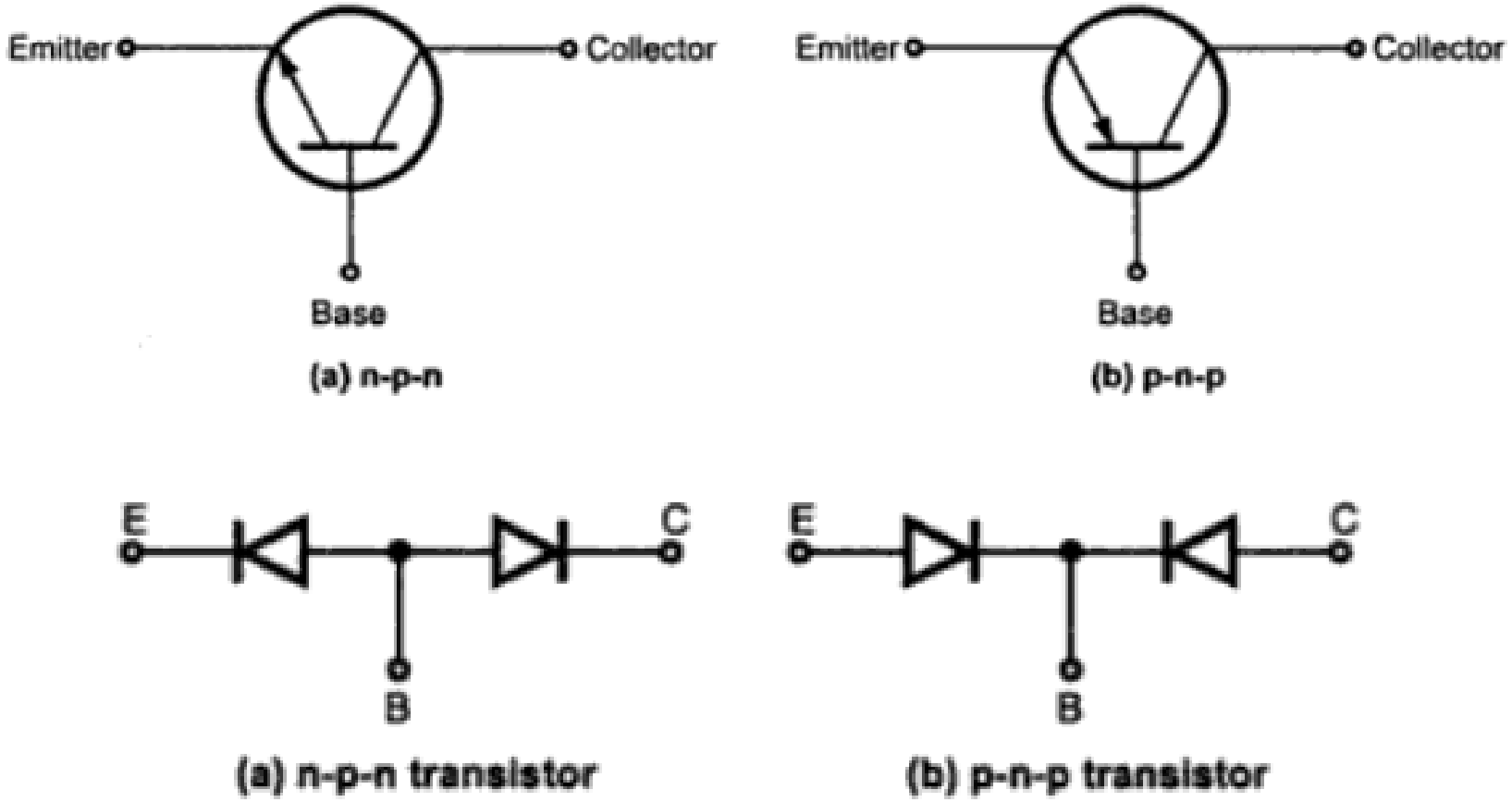


Fig. 4.3 Two-diode transistor analogy

Why 2 diode configuration can not be used as transistor

1. **Relative doping levels in the base, emitter and collector junctions must be satisfied to work that device as a transistor. Two normal p-n junction diodes can not satisfy this requirement.**

2. **In a transistor, emitter to base junction is forward biased while base to collector junction is reversed biased. But due to diffusion process almost entire emitter current reaches to collector and base current is negligibly small. Thus due to diffusion, device works as a transistor. While in back to back connected diodes there are two separate diodes, one forward biased and one reverse biased and diffusion can not take place. Thus maximum series current which can flow is reverse saturation current of a reverse biased diode. Hence the combination of back to back connected diodes can not be used as transistor.**

Diffusion, **process** resulting from random motion of molecules by which there is a net flow of matter from a region of high concentration to a region of low concentration

Transistor operating regions

1) Active region 2) Cut-off region and 3) Saturation region.

Region	Emitter base junction	Collector base junction
Active	Forward biased	Reverse biased
Cut-off	Reverse biased	Reverse biased
Saturation	Forward biased	Forward biased

Working of NPN Transistor

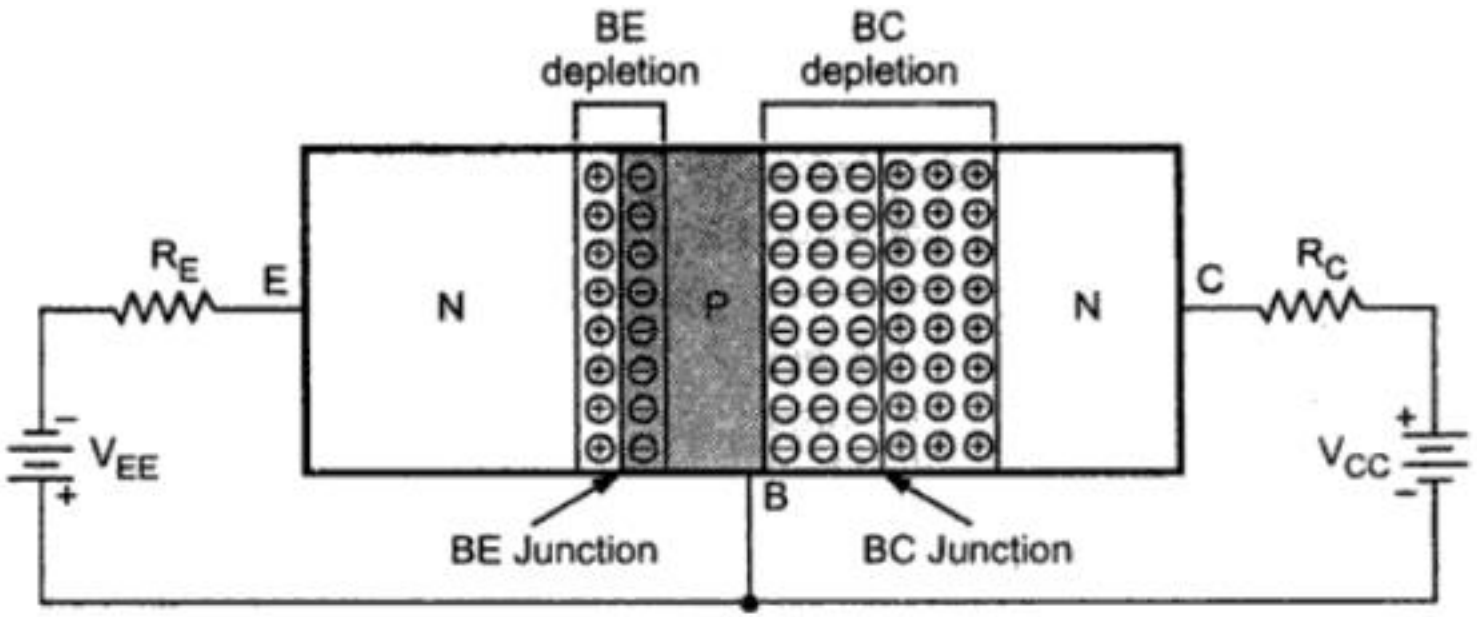


Fig. 4.6 Internal effect of forward biased EB junction and reverse biased CB junction

The forward biased EB junction causes the electrons in the n-type emitter to flow towards the base. This constitutes the emitter current I_E. As these electrons flow through the p-type base, they tend to combine with holes in p-region (base).

We know that, the base region is very thin and lightly doped. The light doping means that the free electrons have a long lifetime in the base region. The very thin base region means that the free electrons have only a short distance to go to reach the collector. For these two reasons, very few of the electrons injected into the base from the emitter recombine with holes to constitute base current, I_B (Refer Fig. 4.7) and the remaining large number of electrons cross the base region and move through the collector region to the positive terminal of the external dc source as shown in Fig. 4.8.

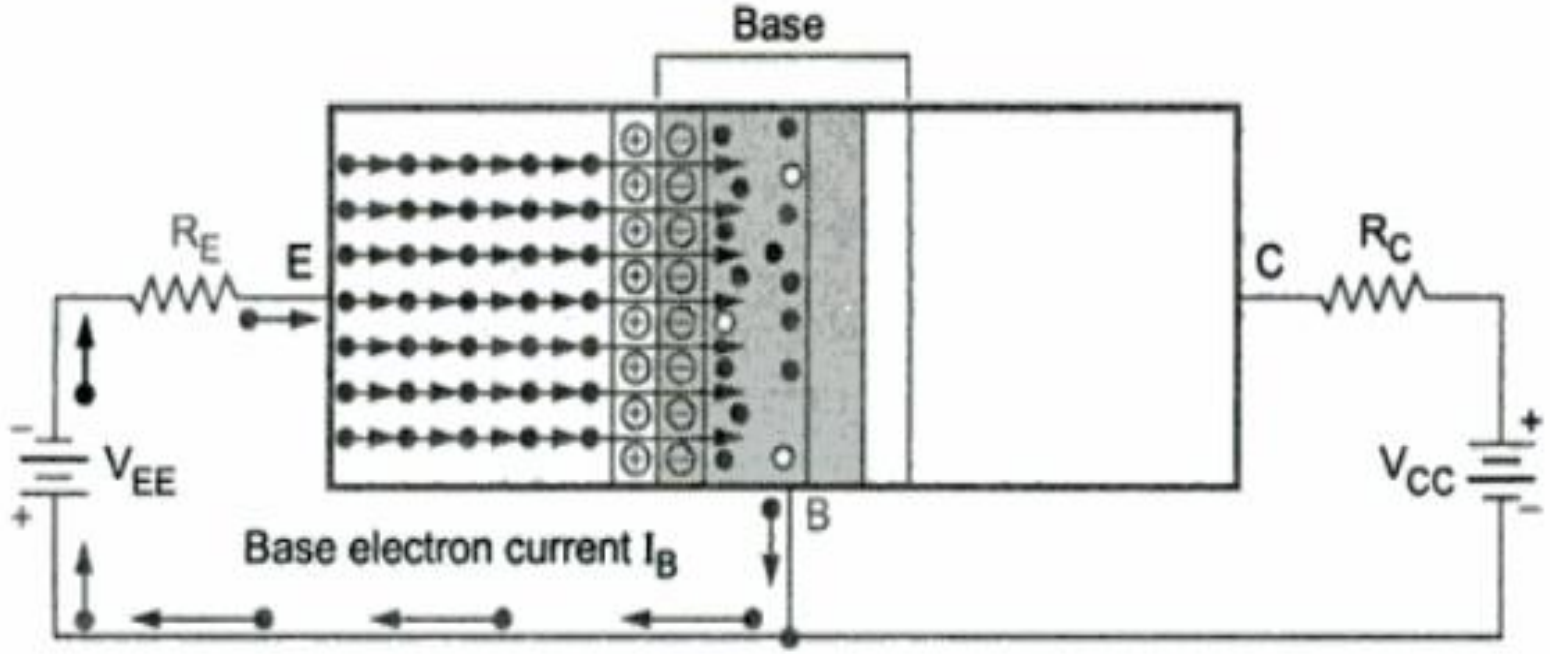


Fig. 4.7 Electron flow across emitter-base junction

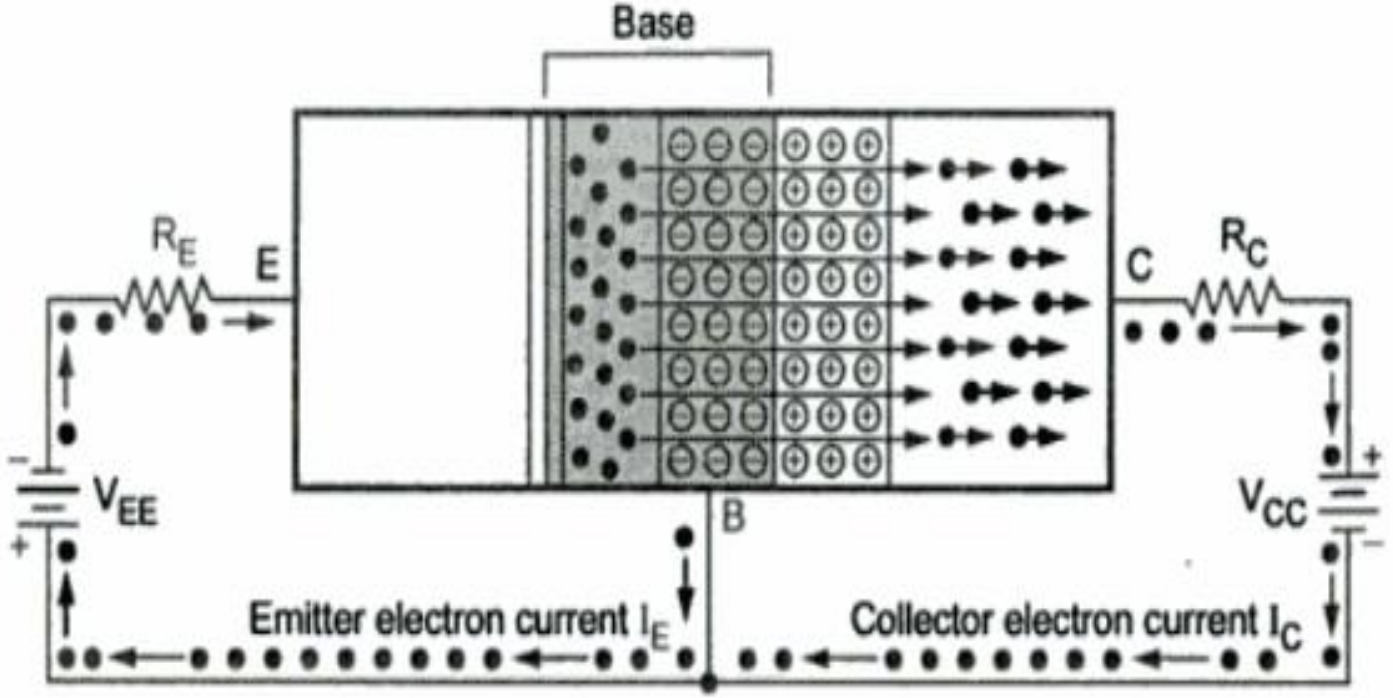


Fig. 4.8 Electron flow across base-collector junction

This constitutes collector current I_C. Thus the electron flow constitutes the dominant current in an npn transistor. Since, the most of the electrons from emitter flow in the collector circuit and very few combine with holes in the base. Thus, the collector current is larger than the base current.

Working of pnp transistor

The p-n-p transistor has its bias voltages V_{EE} and V_{CC} reversed from those in the n-p-n transistor. This is necessary to forward-bias the emitter-base junction and reverse-bias the collector base junction as shown in the Fig. 4.9. The forward biased EB junction causes the holes in the p-type emitter to flow towards the base. This constitutes the emitter current I_E. As these holes flow through the n-type base, they tend to combine with electrons in n-region (base). As the base is very thin and lightly doped, very few of the holes injected into the base from the emitter recombine with electrons to constitute base current, I_B, as shown in the Fig. 4.10.

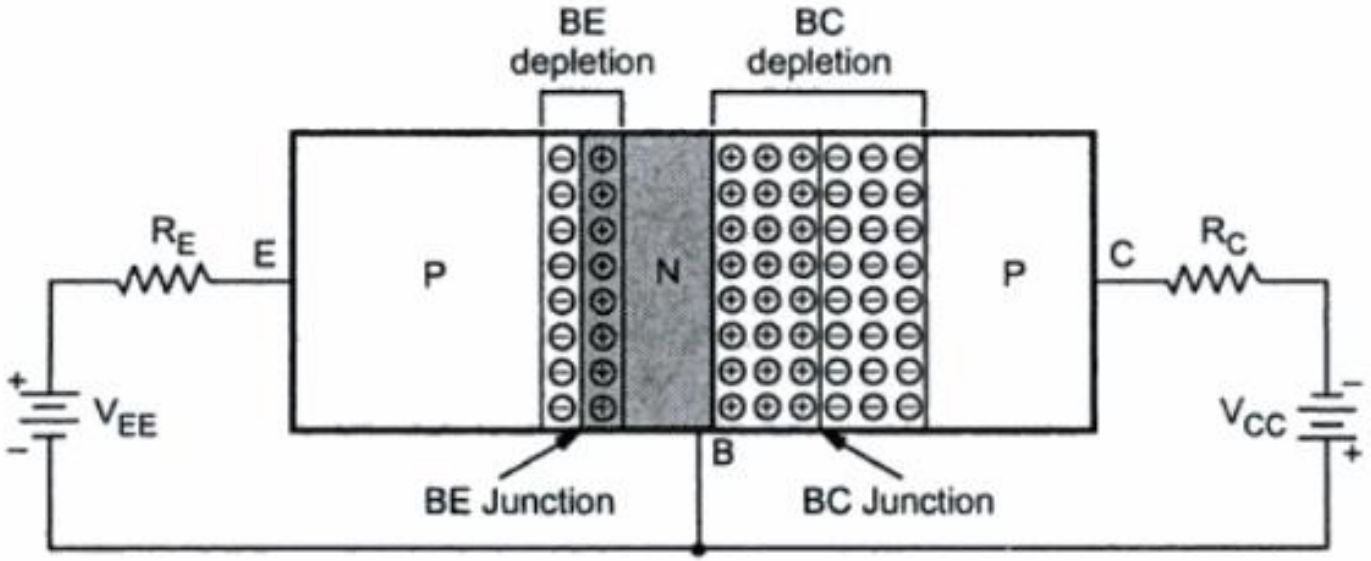


Fig. 4.9 Internal effect of forward biased EB junction and reverse biased CB junction

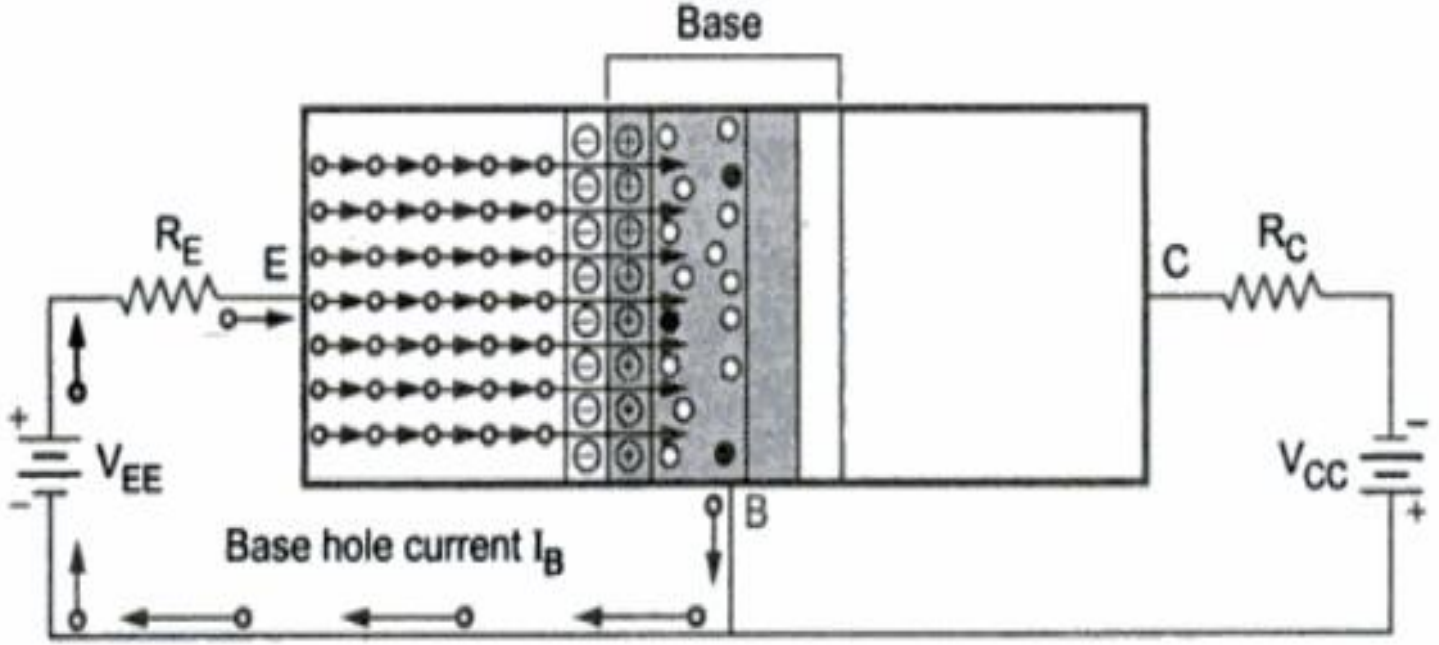


Fig. 4.10 Hole flow across base emitter junction

The remaining large number of holes cross the depletion region and move through the collector region to the negative terminal of the external dc source, as shown in Fig. 4.11. This constitutes collector current I_C. Thus the hole flow consistutes the dominant current in an p-n-p transistor.

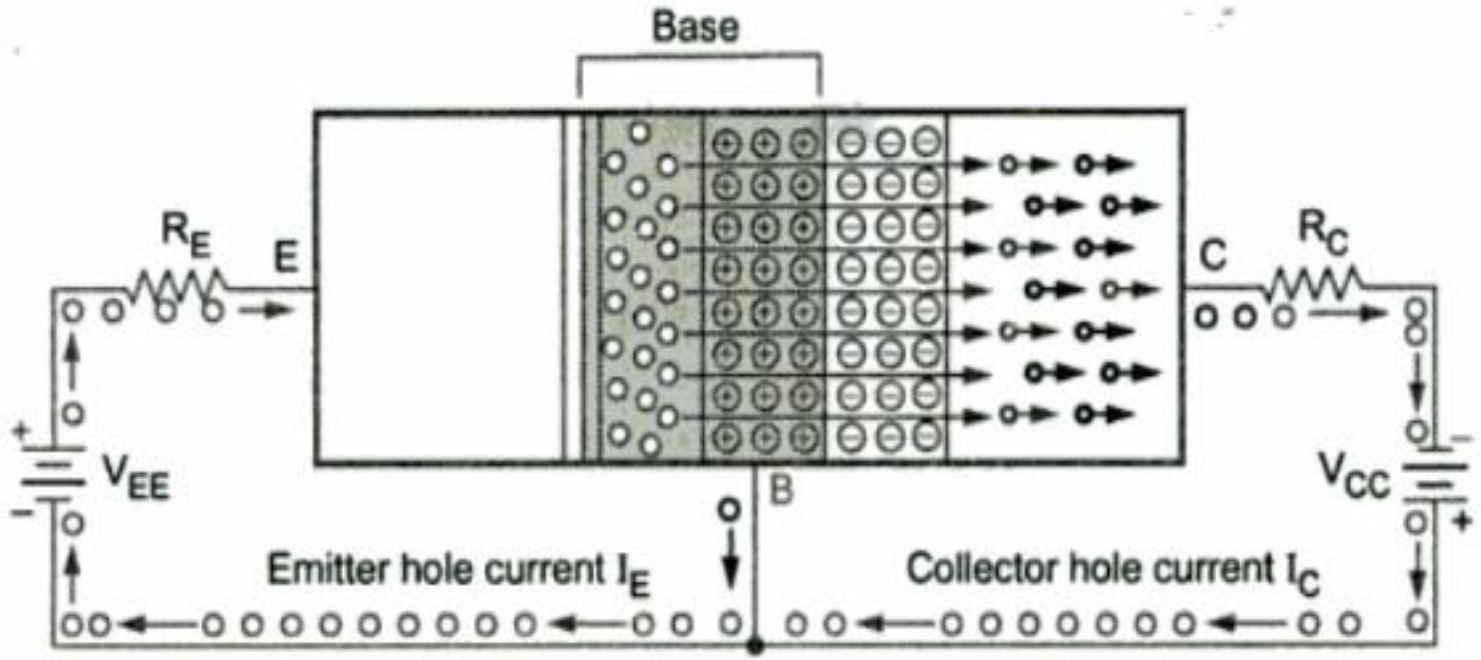


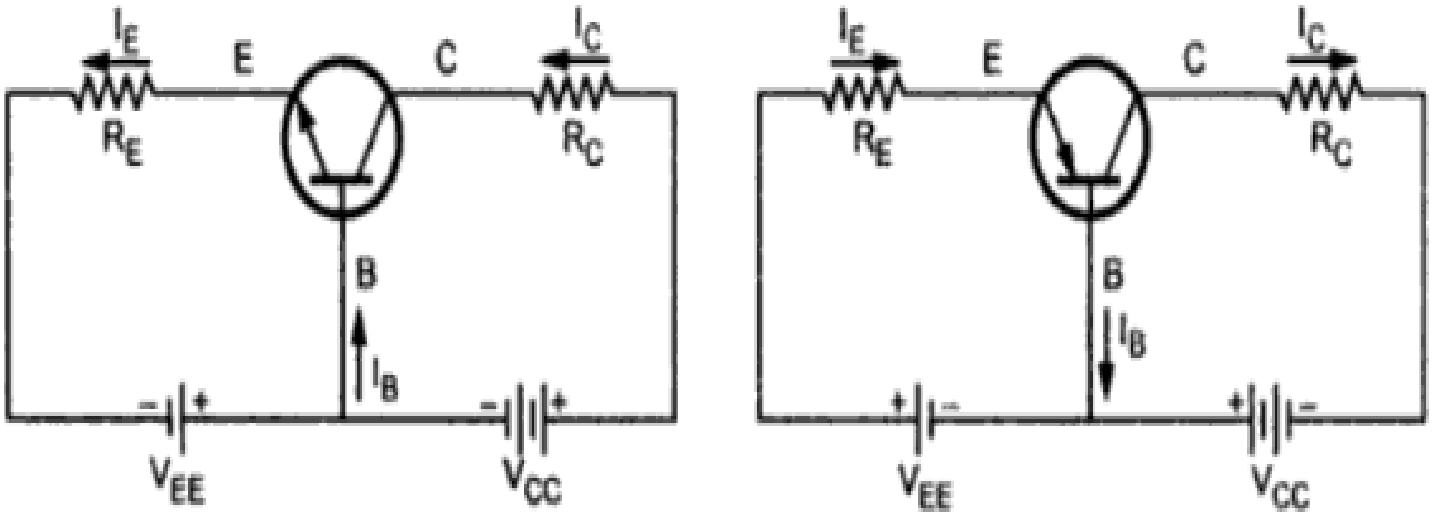
Fig. 4.11 Hole flow across base-collector junction

Transistor configurations:

- CB configuration
- CC configuration
- CE configuration

CB configuration

As shown in Fig. 4.22, in this configuration input is applied between emitter and base and output is taken from the collector and base. Here, base of the transistor is common to both input and output circuits and hence the name common base configuration. Common base configurations for both n-p-n and p-n-p transistors are shown in Fig. 4.22 (a) and 4.22 (b), respectively.



Here, $I_C = \alpha_{dc} I_E + I_{CBO}$

The reverse saturation current, I_{CBO}, is temperature sensitive and it doubles for every 10 °C rise in temperature. Since I_{CBO} is negligibly small in most practical situations, we can approximately write :

$$I_C = \alpha_{dc} I_E$$

or $$\alpha_{dc} = \frac{I_C}{I_E}$$

For a transistor, $I_E = I_B + I_C$

$$\therefore \quad I_E = I_B + (\alpha_{dc} I_E + I_{CBO})$$

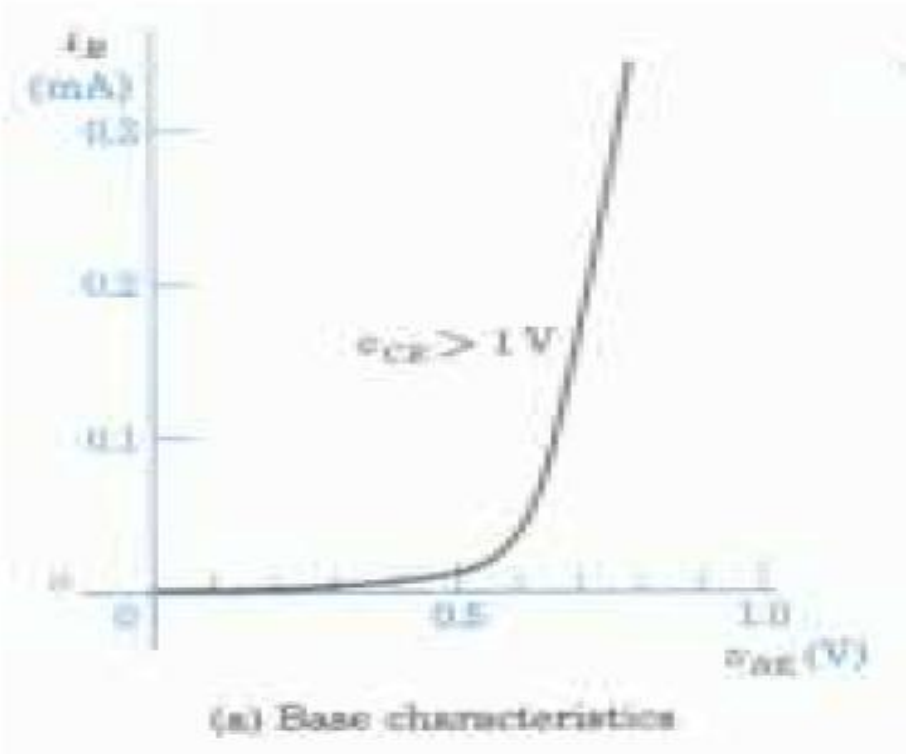
$$\therefore \quad I_B = I_E - (\alpha_{dc} I_E + I_{CBO})$$

$$\therefore \quad \boxed{I_B = (1 - \alpha_{dc}) I_E - I_{CBO}}$$

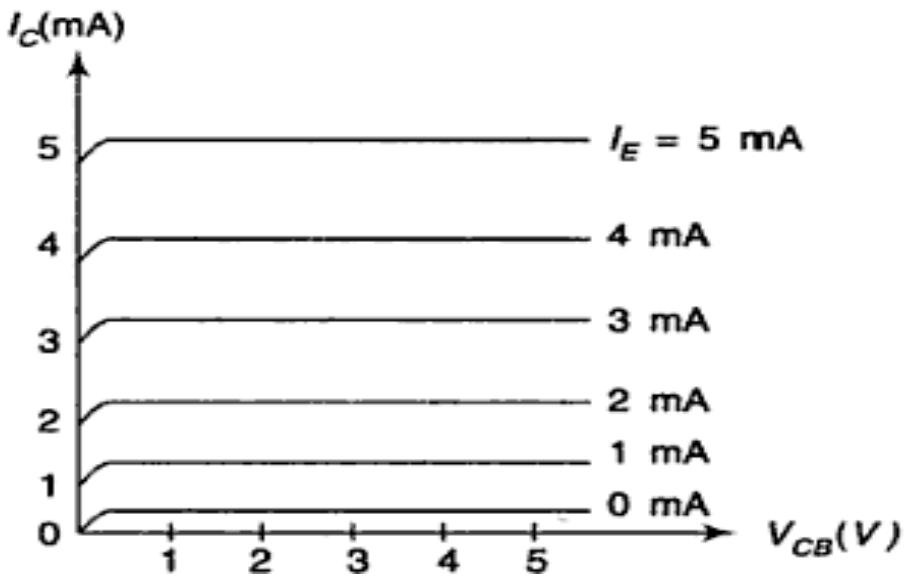
Neglecting I_{CBO} we can write,

$$\therefore \quad \boxed{I_B = (1 - \alpha_{dc}) I_E}$$

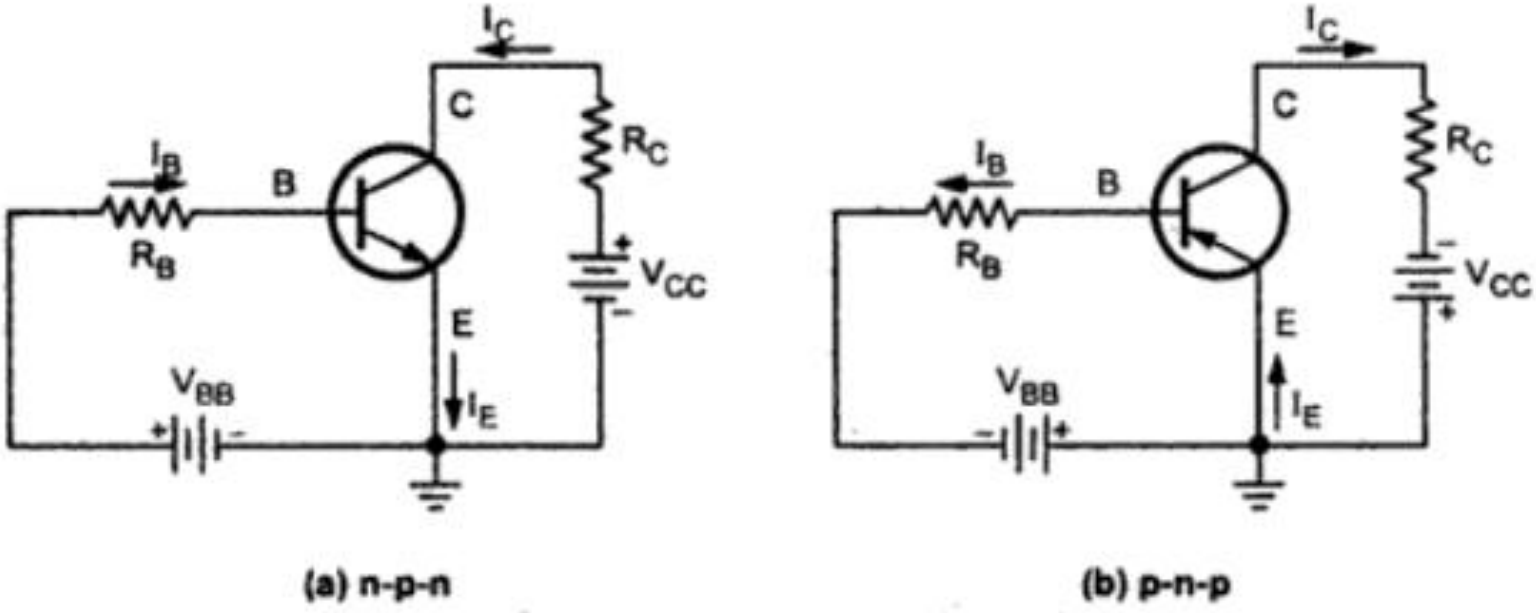
- Input characteristics: The output (CB) V_{BC} voltage is maintained constant and the input voltage (EB) is set at several convenient levels. For each level of input voltage, the input current I_E is recorded. I_E is then plotted versus V_{EB} to give the common-base input characteristics.



- Output characteristics: The emitter current I_E is held constant at each of several fixed levels. For each fixed value of I_E , the output voltage V_{CB} is adjusted in convenient steps and the corresponding levels of collector current I_C are recorded. For each fixed value of I_E, I_C is almost equal to I_E and appears to remain constant when V_{CB} is increased



CE configuration



(a) n-p-n (b) p-n-p

Fig. 4.29 Common emitter configurations

Calculation of input(I_B) and output currents(I_C)

We have seen $$I_C = \alpha_{dc} I_E + I_{CBO}$$

$$\therefore \quad I_C - I_{CBO} = \alpha_{dc} I_E$$

Dividing by α_{dc}, $$\frac{I_C}{\alpha_{dc}} - \frac{I_{CBO}}{\alpha_{dc}} = I_B + I_C$$

$$\therefore \quad I_C\left[\frac{1}{\alpha_{dc}} - 1\right] = I_B + \frac{I_{CBO}}{\alpha_{dc}}$$

$$I_C\left[\frac{1-\alpha_{dc}}{\alpha_{dc}}\right] = I_B + \frac{I_{CBO}}{\alpha_{dc}}$$

$$\therefore \quad I_C = \left(\frac{\alpha_{dc}}{1-\alpha_{dc}}\right) I_B + \left(\frac{1}{1-\alpha_{dc}}\right) I_{CBO}$$

Now we define a new parameter "beta" (β_{dc}) for the transistor as :

$$\boxed{\beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}}}$$

It is also known as h_{fe}.

In terms of 'β', the equation for I_C becomes

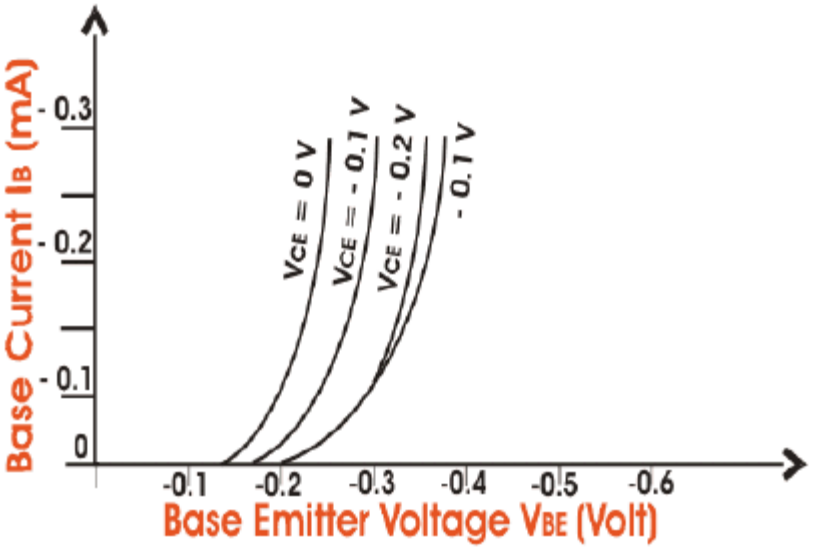
$$I_C = \beta_{dc} I_B + [1 + \beta_{dc}] I_{CBO} \quad \because 1 + \beta_{dc} = \frac{1}{1 - \alpha_{dc}}$$

The term "$(\beta_{dc}+1) I_{CBO}$" is the **reverse leakage current** in common-emitter configuration. It is designated as I_{CEO}.

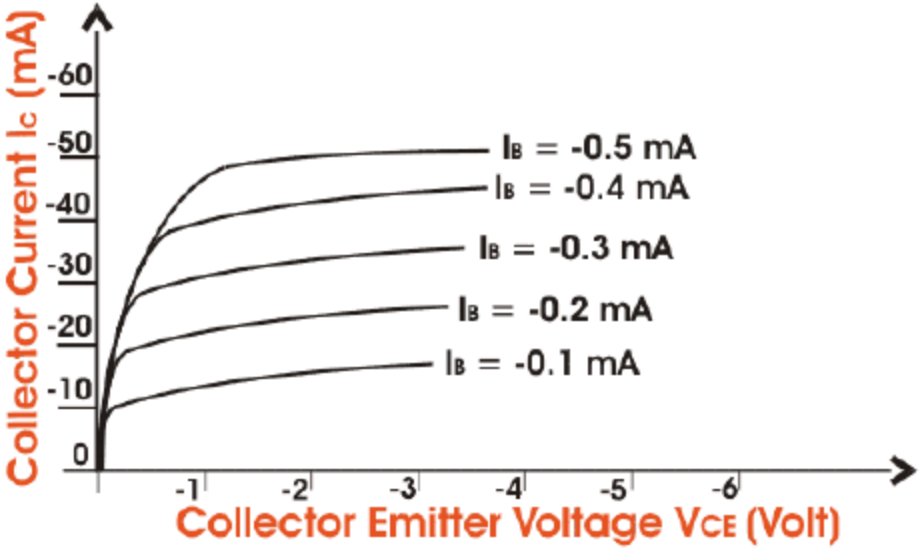
$$\boxed{I_{CEO} = (\beta_{dc}+1) I_{CBO}}$$

$\because I_B << I_C$

- Input characteristics: The output voltage V_{CE} is maintained constant and the input voltage V_{BE} is set at several convenient levels. For each level of input voltage, the input current I_B is recorded. I_B is then plotted versus V_{BE} to give the common-base input characteristics.



- Output characteristics: The Base current I_B is held constant at each of several fixed levels. For each fixed value of I_B , the output voltage V_{CE} is adjusted in convenient steps and the corresponding levels of collector current I_C are recorded. For each fixed value of I_B, I_C level is Recorded at each V_{CE} step. For each I_B level, I_C is plotted versus V_{CE} to give a family of characteristics.



CC configuration

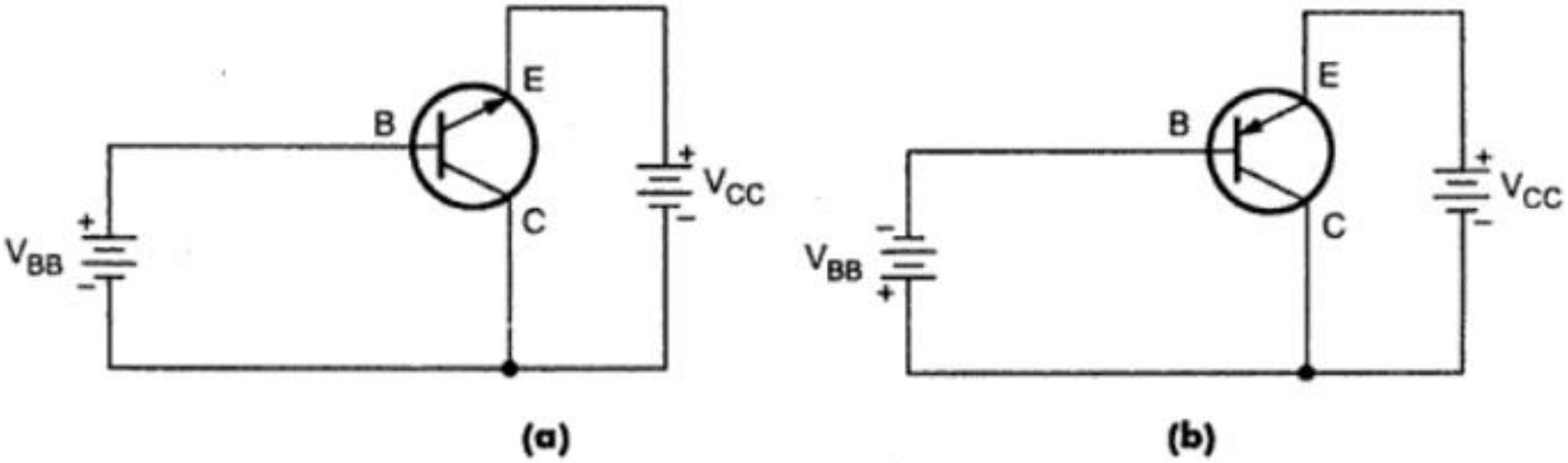


Fig. 4.36 Common collector configurations

Calculation of input(I_B) and output currents(I_E)

In CC configuration, I_B is the input current and the I_E is the output current. Now we are interested in knowing how the output current I_E is related with the input current I_B.

We have $$I_E = I_B + I_C \quad \ldots (1)$$

Here we are not interested in I_C and we know that $I_C = \alpha I_E + I_{CBO}$ by substituting value of I_C in equation (1) we get,

$$I_E = I_B + \alpha_{dc} I_E + I_{CBO}$$

Or $$(1 - \alpha_{dc}) I_E = I_B + I_{CBO}$$

Or $$I_E = \frac{1}{1 - \alpha_{dc}} I_B + \frac{1}{1 - \alpha_{dc}} I_{CBO} \quad \ldots (2)$$

We know $$\beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}}$$

$$\therefore \quad 1+\beta_{dc} = \frac{1-\alpha_{dc}+\alpha_{dc}}{1-\alpha_{dc}} = \frac{1}{1-\alpha_{dc}}$$

Now by substituting $1+\beta_{dc}$ instead of $\frac{1}{1-\alpha_{dc}}$ in equation (2), we get,

$$I_E = (1+\beta_{dc})\, I_B + (1+\beta_{dc})\, I_{CBO}$$

If we neglect the leakage current I_{CBO} then

$$I_E = (1+\beta_{dc})\, I_B$$

$$\therefore \quad \boxed{\frac{I_E}{I_B} = (1+\beta_{dc})}$$

Input characteristics To determine the input characteristics, V_{EC} is kept at a suitable fixed value. The base-collector voltage V_{BC} is increased in equal steps and the corresponding increase in I_B is noted. This is repeated for different fixed values of V_{EC}. Plots of V_{BC} versus I_B for different values of V_{EC} shown in Fig. 6.14 are the input characteristics.

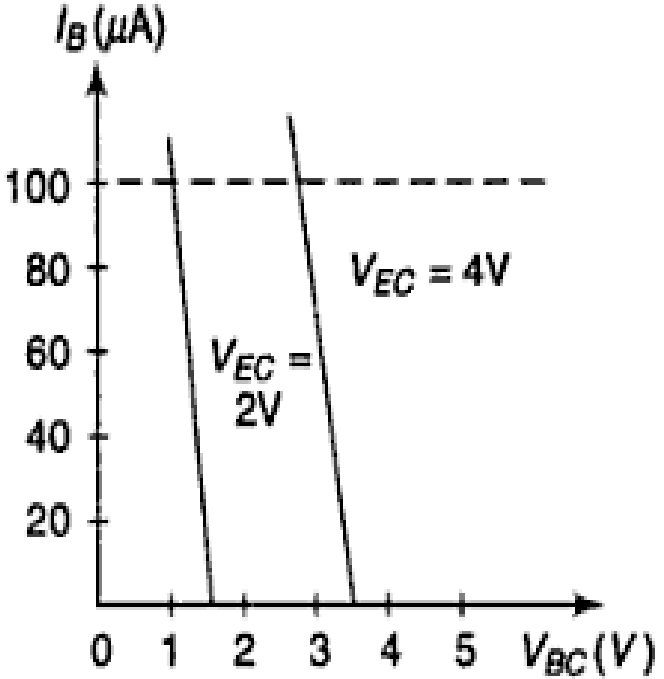


Fig. 6.14 CC input characteristics

Output characteristics The output characteristics shown in Fig. 6.15 are the same as those of the common emitter configuration.

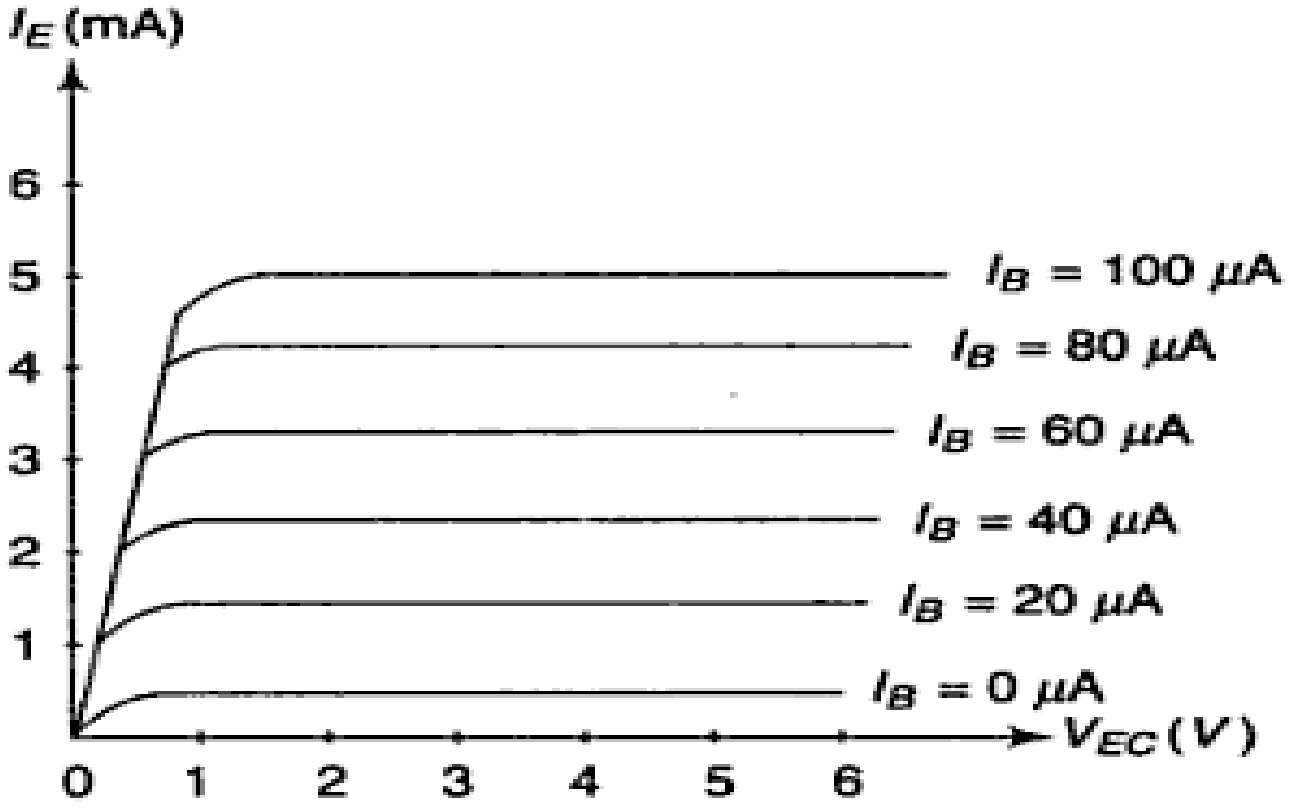


Fig. 6.15 CC output characteristics

WHY CE CONFIGURATION IS USED IN AMPLIFIERS

- IT provides both voltage and current gain more than unity
- Ratio of output resistance to input resistance is very small(10 to 100ohms)

Sr.No.	Characteristic	Common Base	Common Emitter	Common Collector
1.	Input resistance	Very low (20Ω)	Low (1kΩ)	High (500 kΩ)
2.	Output resistance	Very high (1MΩ)	High (40kΩ)	Low (50Ω)
3.	Input current	I_E	I_B	I_B
4.	Output current	I_C	I_C	I_E
5.	Input voltage applied between	Emitter and Base	Base and Emitter	Base and Collector
6.	Output voltage taken between	Collector and Base	Collector and Emitter	Emitter and Collector
7.	Current amplification factor	$\alpha_{dc} = \frac{I_C}{I_E}$	$\beta_{dc} = \frac{I_C}{I_B}$	$\frac{I_E}{I_B}$
8.	Current gain	Less than unity	High (20 to few hundreds)	High (20 to few hundreds)
9.	Voltage gain	Medium	Medium	Low
10.	Applications	As a input stage of multistage amplifier	For audio signal amplification	For impedance matching

Relation between alpha & beta

We know that

$$\beta = \frac{I_C}{I_B} \quad \ldots (1)$$

$$\alpha = \frac{I_C}{I_E} \quad \ldots (2)$$

Now, $i_E = I_C + I_B$

Or $I_B = I_E - I_C$

Substituting the value of I_B in equation (1) we get,

$$\beta = \frac{I_C}{I_E - I_C} \quad \ldots (3)$$

Dividing the numerator and denominator of R.H.S. of equation (3) by I_E, we get,

$$\beta = \frac{\frac{I_C}{I_E}}{\frac{I_E}{I_E} - \frac{I_C}{I_E}}$$

We know that, $\alpha = \frac{I_C}{I_E}$ from equation (2)

$$\therefore \quad \beta = \frac{\alpha}{1-\alpha} \qquad \ldots (4)$$

b) Dividing the R.H.S. and L.H.S. by $1 + \beta$ we get,

$$\frac{\beta}{1+\beta} = \frac{\frac{\alpha}{1-\alpha}}{1+\beta}$$

By substituting value of β from equation (4) in R.H.S. we get,

$$\frac{\beta}{1+\beta} = \frac{\frac{\alpha}{1-\alpha}}{1+\frac{\alpha}{1-\alpha}} \quad \Rightarrow \quad \frac{\beta}{1+\beta} = \frac{\frac{\alpha}{1-\alpha}}{\frac{1-\alpha+\alpha}{1-\alpha}}$$

Cancelling common denominator terms we get,

$$\frac{\beta}{1+\beta} = \frac{\alpha}{1-\alpha+\alpha} = \alpha$$

$$\therefore \quad \alpha = \frac{\beta}{1+\beta}$$

BJT BIASING

- Biasing is the process of providing DC voltage which helps in the functioning of the circuit.

- A transistor is based in order to make the emitter base junction forward biased and collector base junction reverse biased, so that it maintains in active region, to work as an amplifier.

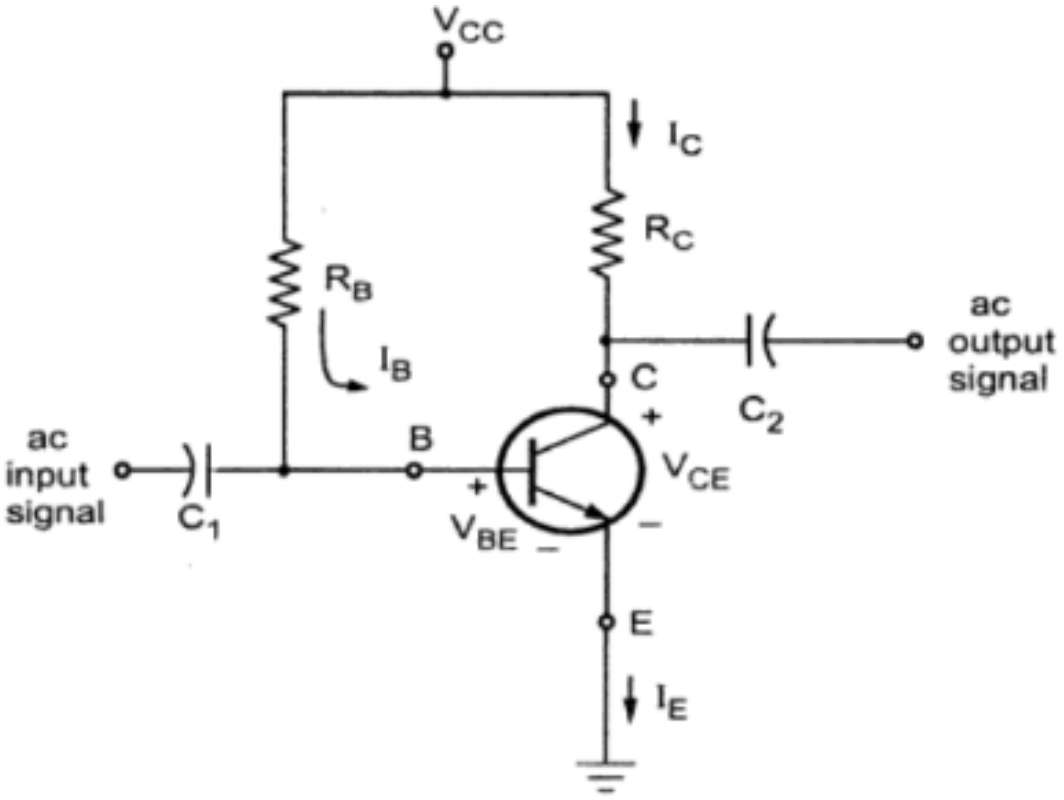
NEED OF BIASING

- If a signal of very small voltage is given to the input of BJT, it cannot be amplified. Because, for a BJT, to amplify a signal, two conditions have to be met.

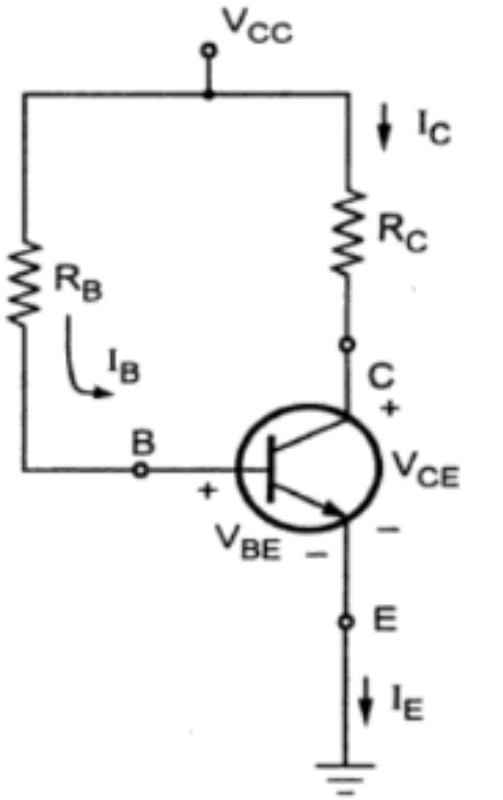
  - The input voltage should exceed **cut-in voltage** for the transistor to be **ON**.
  - The BJT should be in the **active region**, to be operated as an **amplifier**.

- If appropriate DC voltages and currents are given through BJT by external sources, so that BJT operates in active region and superimpose the AC signals to be amplified, then this problem can be avoided. The given DC voltage and currents are so chosen that the transistor remains in active region for entire input AC cycle. Hence DC biasing is needed

FIXED BIAS

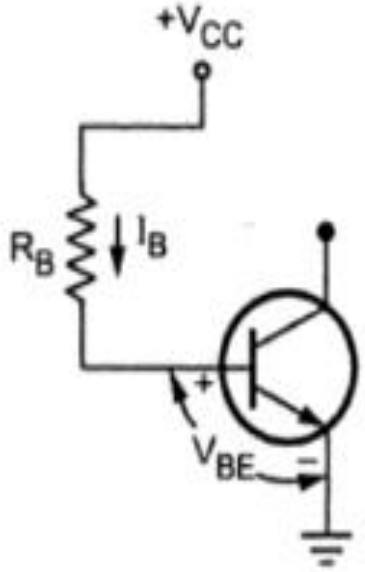


(a) Fixed bias circuit



(b) D.C. equivalent of Fig (a)

Base circuit of the fixed bias circuit



Base Circuit :

Let us consider the base circuit as shown in Fig. 1.9.

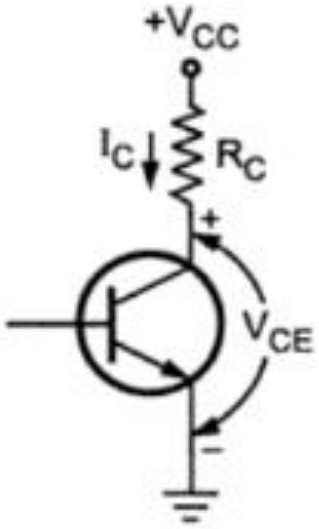
Applying Kirchhoff's voltage law to the base circuit we get,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

Solving for the current I_B,

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B}} \quad \ldots (1)$$

Collector circuit of the fixed bias circuit



Collector Circuit

We now consider the collector circuit as shown in Fig. 1.10. Applying Kirchhoff's voltage law to the collector circuit we get,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\therefore \quad \boxed{V_{CE} = V_{CC} - I_C R_C} \qquad \ldots (2)$$

The magnitude of collector current is given by,

$$\therefore \quad \boxed{I_C = \beta I_B} \qquad \ldots (3)$$

and from equation 2 we have,

$$\boxed{I_C = \frac{V_{CC} - V_{CE}}{R_C}} \qquad \ldots (4)$$

It is important to note that since the base current is controlled by the value of R_B and I_C is related to I_B by a constant β, the magnitude of I_C is not a function of the resistance R_C. Changing R_C to any level will not affect the level of I_B or I_C as long as we remain in the active region of the device. However, the change in R_C will change the value of V_{CE}.

$$\boxed{V_{CE} = V_C - V_E} \qquad \ldots (5)$$

Similarly,

$$\boxed{V_{BE} = V_B - V_E} \quad \ldots (6)$$

Where, V_B : Base voltage

In this circuit, $V_E = 0$,

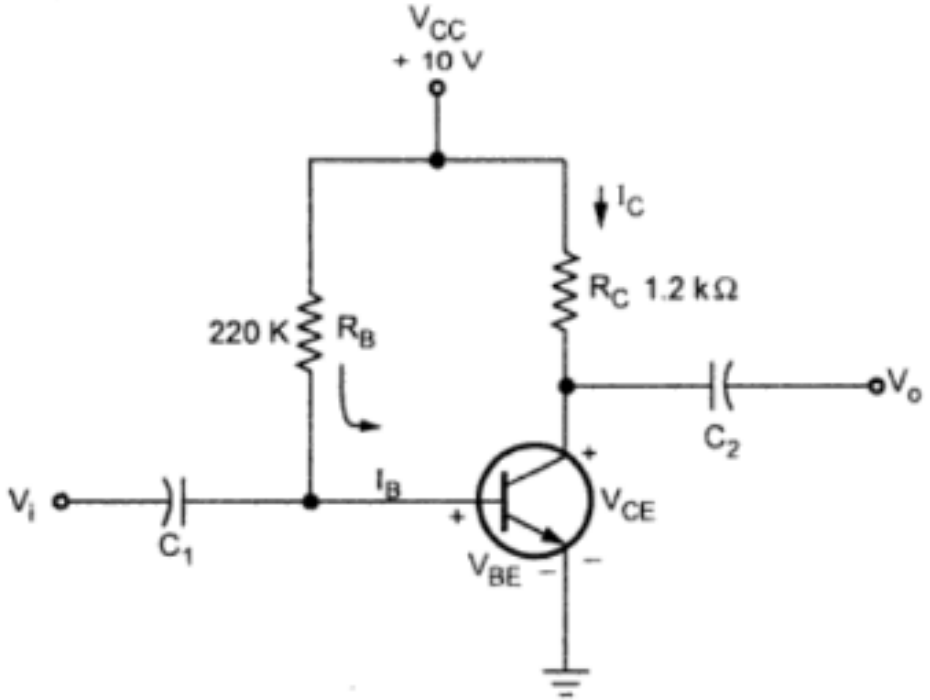
$$\therefore \quad \boxed{V_{BE} = V_B} \quad \ldots (7)$$

and

$$\boxed{V_{CE} = V_C} \quad \ldots (8)$$

Example 1.1 : *For the circuit shown in the Fig. 1.11. Calculate* $I_B, I_C, V_{CE}, V_B, V_C$ *and* V_{BC}. *Assume* $V_{BE} = 0.7\,V$ *and* $\beta = 50$.

Figure 1.11



Solution :

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{10 - 0.7}{220 \times 10^3} = \mathbf{42.27\ \mu A}$$

$$I_C = \beta I_B = 50 \times 42.27 \times 10^{-6} = \mathbf{2.1135\ mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 10 - 2.1135 \times 10^{-3} \times 1.2 \times 10^3$$

$$= \mathbf{7.4638\ V}$$

$$V_B = V_{BE} = \mathbf{0.7\ V}$$

$$V_C = V_{CE} = \mathbf{7.4638\ V}$$

$$V_{BC} = V_B - V_C = 0.7 - 7.4638 = \mathbf{-6.7638}$$

The negative voltage V_{BC} indicates that base-collector junction is reverse biased.

DC LOAD LINE

For fixed-bias circuit, we have

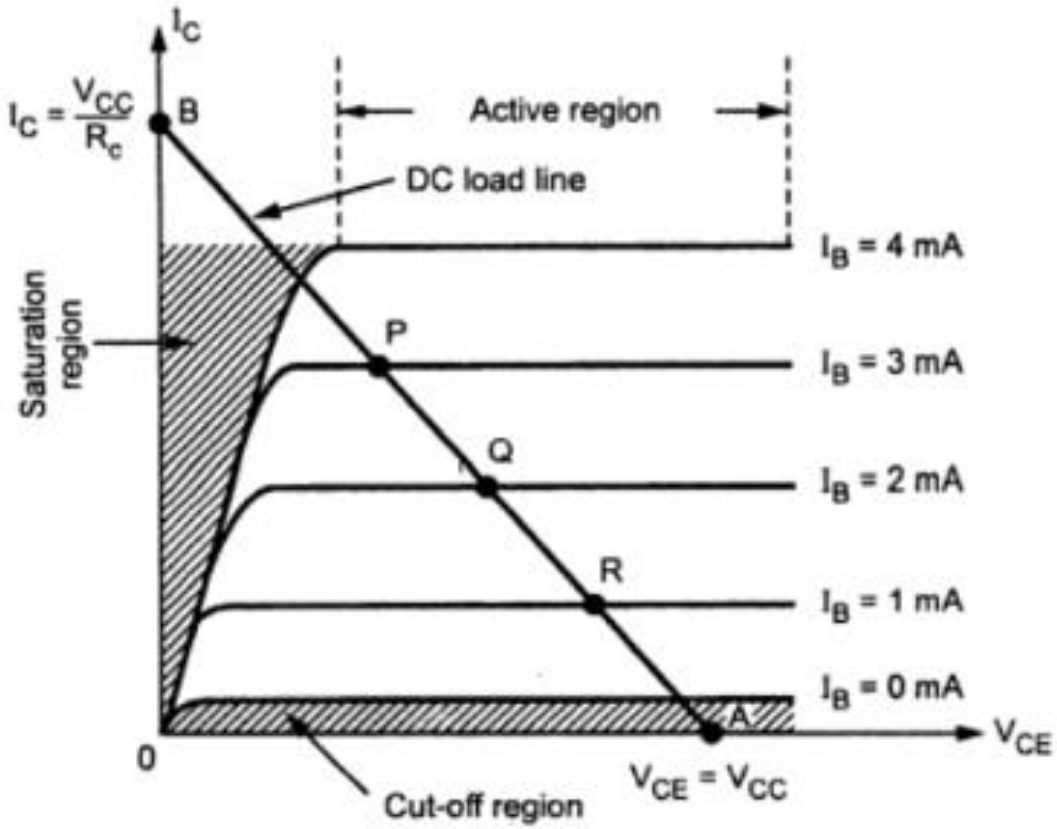
$$I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{V_{CC}}{R_C} - \left[\frac{1}{R_C}\right] V_{CE}$$

$$= -\left[\frac{1}{R_C}\right] V_{CE} + \frac{V_{CC}}{R_C}$$

By comparing this equation with equation of straight line $y = mx + c$, where m is the slope of the line and c is the intercept on Y-axis, then we can draw a straight line on the graph of I_C versus V_{CE} which is having slope $-1/R_C$ and Y-intercept V_{CC}/R_C. To determine the two points on the line we assume $V_{CE} = V_{CC}$ and $V_{CE} = 0$.

a) When $V_{CE} = V_{CC}$; $I_C = 0$ and we get a point A and

b) When $V_{CE} = 0$; $I_C = V_{CC}/R_C$ and we get a point B



The Fig. 1.12 shows the output characteristics of a common emitter configuration with points A and B, and line drawn between them. The line drawn between points A and B is called **d.c. load line**. The 'd.c.' word indicates that only d.c. conditions are considered, i.e. input signal is assumed to be zero.

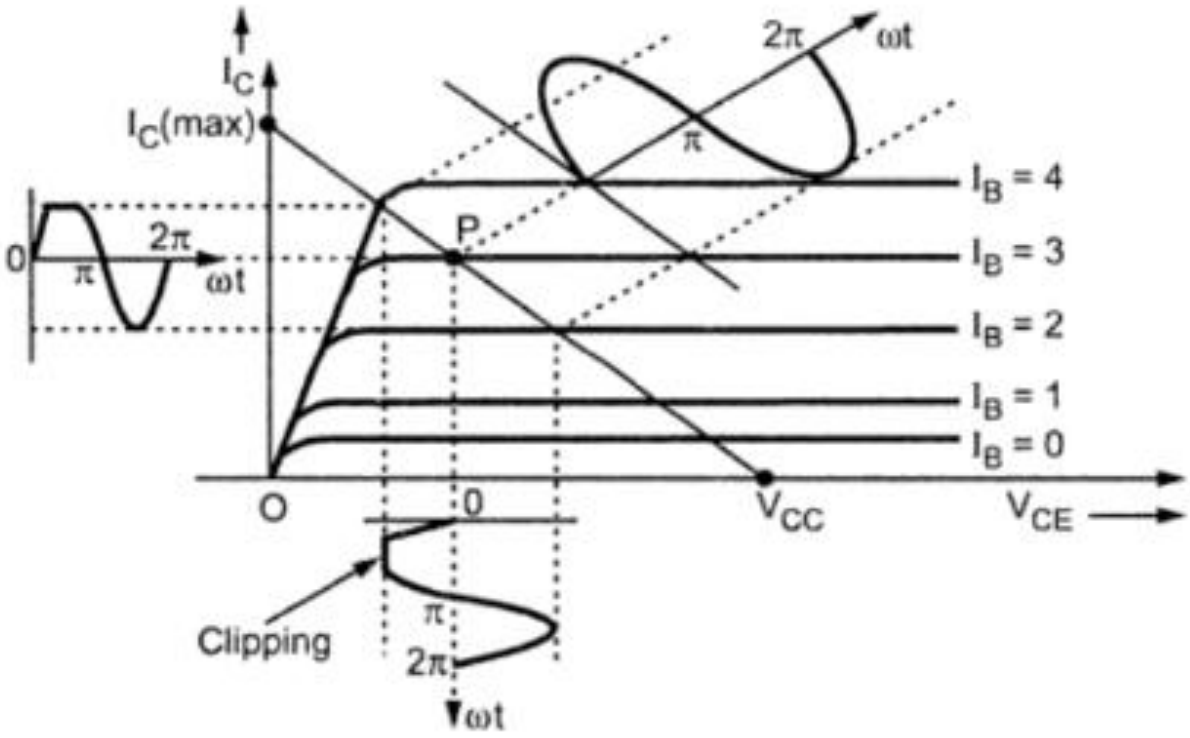
The d.c. load line is a plot of I_C versus V_{CE}. For a given value of R_C and a given level of V_{CC}. Thus, it represents all collector current levels and corresponding collector-emitter voltages that can exist in the circuit. Knowing any one of I_C, I_B or V_{CE}, it is easy to determine the other two from the load line. The slope of the d.c. load line depends on the value of R_C. It is negative and equal to reciprocal of the R_C.

SELECTING OPERATING POINT

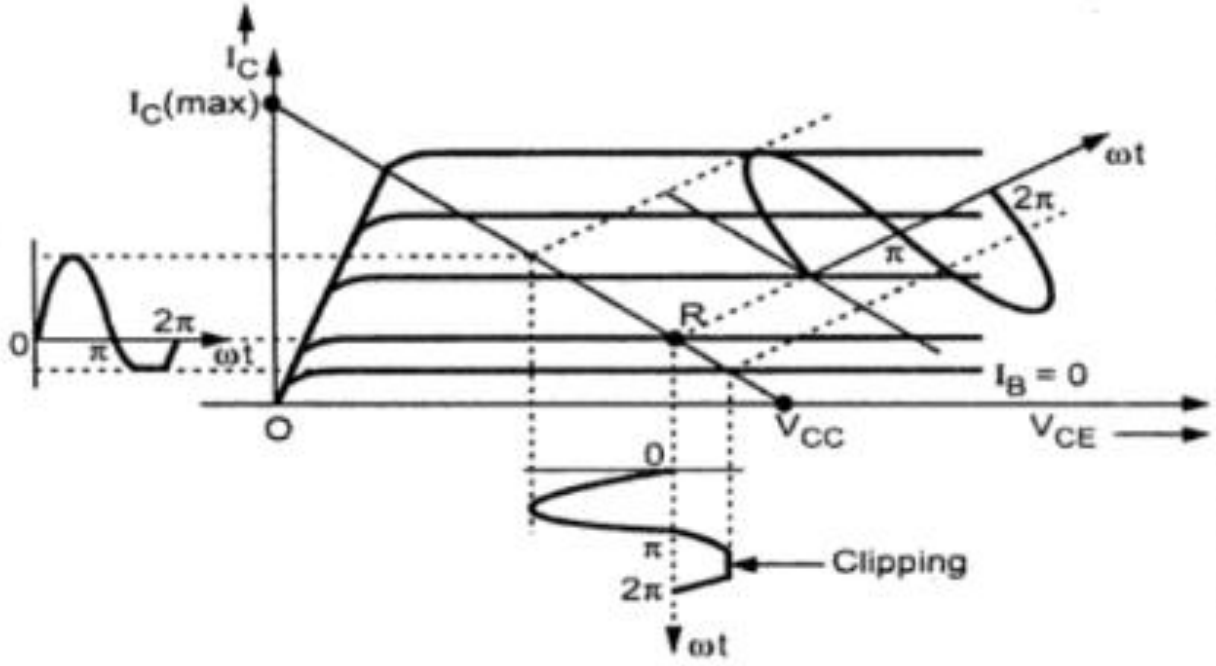
The operating point can be selected at different positions on the d.c. load line : near saturation region, near cut-off region or at the center, i.e. in the active region. Refer Fig. 1.13. The selection of operating point will depend on its application. When transistor is used as an amplifier, the Q point should be selected at the center of the d.c. load line to prevent any possible distortion in the amplified output signal. This is well-understood by going through following cases.

Case 1 : Biasing circuit is designed to fix a Q point at point P, as shown in Fig. 1.14. Point P is very near to the saturation region. As shown in Fig. 1.14 the collector current is clipped at the positive half cycle. So, eventhough base current varies sinusoidally, collector current is not a useful sinusoidal waveform. i.e. distortion is present at the output. Therefore, point P is not a suitable operating point.

Operating point near saturation region gives clipping at the positive peaks

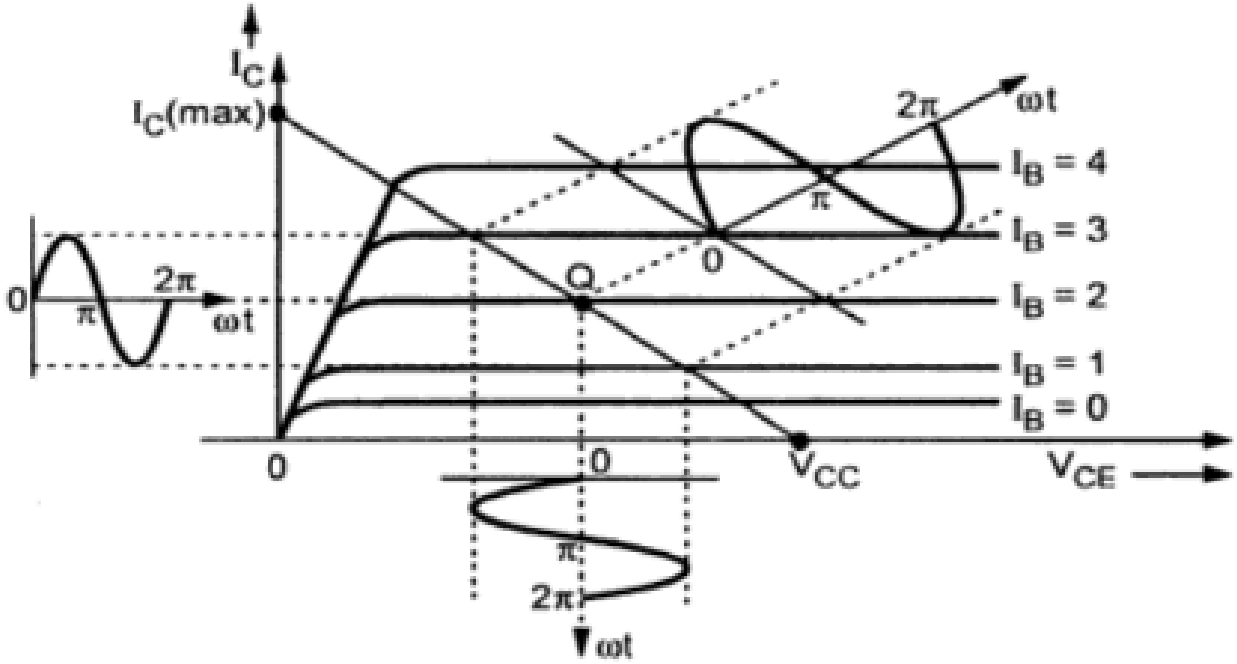


Operating point near cut-off region gives clipping at the negative peaks



Case 2 : Biasing circuit is designed to fix a Q point at point R as shown in Fig. 1.15. Point R is very near to the cut-off region. As shown in Fig. 1.15 the collector current is clipped at the negative half cycle. So, point R is also not a suitable operating point.

Operating point at the centre of active region is most suitable



Case 3 : Biasing circuit is designed to fix a Q point at point Q as shown in Fig. 1.16. The output signal is sinusoidal waveform without any distortion. Thus point Q is the best operating point.

VARIATION OF Q-POINT

Two important factors are to be considered while designing the biasing circuit which are responsible for shifting the operating point.

I) Temperature

1) I_{CO} : The flow of current in the circuit produces heat at the junctions. This heat increases the temperature at the junctions. We know that the minority carriers are temperature dependent. They increase with the temperature. The increase in the minority carriers increases the leakage current I_{CEO},

$$\because \quad I_{CEO} = (1 + \beta)\, I_{CBO} \qquad \ldots (9)$$

Specifically, I_{CBO} doubles for every 10°C rise in temperature. Increase in I_{CEO} in turn increases the collector current,

$$\because \quad I_C = \beta\, I_B + I_{CEO} \qquad \ldots (10)$$

2) V_{BE} : Base to emitter voltage V_{BE} changes with temperature at the rate of 2.5 mV/°C. Base current, I_B depends upon V_{BE}. As base current I_B depends on V_{BE} and I_C depends on I_B, I_C depends on V_{BE}. Therefore collector current I_C changes with temperature due to change in V_{BE}. The change in collector current change the operating point.

3) β_{dc} : β_{dc} of the transistor is also temperature dependent. As β_{dc} varies, I_C also varies, since $I_C = \beta I_B$. The change in collector current change the operating point.

REQUIREMENTS OF BIASING CIRCUITS

i) The emitter-base junction must be forward biased (forward biased voltage 0.6 V to 0.7 V) and collector-base junction must be reverse biased (within maximum limits). i.e. the transistor should be operated in the middle of the active region or operating point (Q point) should be fixed at the center of the active region.

ii) The circuit design should provide a degree of temperature stability.

iii) The operating point should be made independent of the transistor parameters (such as β).

ADVANTAGES OF FIXED BIAS

- IT IS SIMPLE IN CONSTRUCTION
- Q POINT CAN BE PLACED ANYWHERE IN ACTIVE REGION BY ADJUSTING VALUE OF R_B

Disadvantages

- The circuit does not provide a check on I_C which increases with temperature.

$$I_C = \beta I_B + I_{CEO}$$

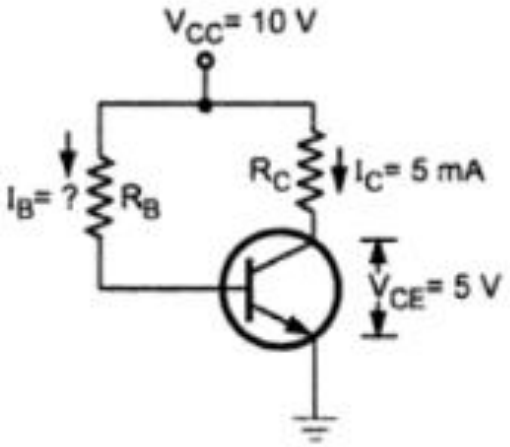
- Since I_B & I_C are fixed change in beta shifts operating point.

$$I_C = \beta I_B$$

Example 1.4 : *Design a fixed biased circuit using a silicon transistor having β value of 100. V_{CC} is 10 V and dc bias conditions are to be V_{CE} = 5 V and I_C = 5 mA.*

Solution :

Figure 1.20



Applying KVL to collector circuit we get,

$$V_{CC} - V_{CE} - I_C R_C = 0$$

$$\therefore R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{10 - 5}{5\,mA} = 1\ K$$

$$I_B = \frac{I_C}{\beta} = \frac{5\,mA}{100} = 50\ \mu A$$

Now, applying KVL to base circuit we get,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{10 - 0.7}{50\,\mu A} = 186\ k\Omega$$

STABILITY FACTOR

- It indicates the degree of change in operating point due to variation in temperature.
- There are 3 variables that are temperature dependant

we can define three stability factors as below :

i) $$S = \left.\frac{\partial I_C}{\partial I_{CO}}\right|_{V_{BE},\ \beta \text{ constant}} \quad \text{or} \quad S = \left.\frac{\Delta I_C}{\Delta I_{CO}}\right|_{V_{BE},\ \beta \text{ constant}} \qquad \ldots (1)$$

ii) $$S' = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO},\ \beta \text{ constant}} \quad \text{or} \quad S' = \left.\frac{\Delta I_C}{\Delta V_{BE}}\right|_{I_{CO},\ \beta \text{ constant}} \qquad \ldots (2)$$

iii) $$S'' = \left.\frac{\partial I_C}{\partial \beta}\right|_{I_{CO},\ V_{BE} \text{ constant}} \quad \text{or} \quad S'' = \left.\frac{\Delta I_C}{\Delta \beta}\right|_{I_{CO},\ V_{BE} \text{ constant}} \qquad \ldots (3)$$

STABILITY FACTOR (S)

For a common emitter configuration collector current is given as,

$$I_C = \beta I_B + I_{CEO}$$

or

$$I_C = \beta I_B + (1+\beta) I_{CBO} \quad \ldots (4)$$

When I_{CBO} changes by ΔI_{CBO}, I_B changes by ∂I_B and I_C changes by ∂I_C . So this equation becomes,

$$\partial I_C = \beta \partial I_B + (1+\beta) \partial I_{CBO}$$

$$\therefore 1 = \beta \frac{\partial I_B}{\partial I_C} + (1+\beta) \frac{\partial I_{CBO}}{\partial I_C}$$

$$\therefore \quad 1 - \beta \frac{\partial I_B}{\partial I_C} = (1+\beta) \frac{\partial I_{CBO}}{\partial I_C}$$

$$\therefore \quad 1 - \beta \frac{\partial I_B}{\partial I_C} = (1+\beta) \frac{\partial I_{CBO}}{\partial I_C}$$

$$\therefore \frac{\partial I_{CBO}}{\partial I_C} = \frac{1 - \beta (\partial I_B / \partial I_C)}{1+\beta}$$

$$S = \frac{\partial I_C}{\partial I_{CBO}}$$

$$S = \frac{(1+\beta)}{1 - \beta (\partial I_B / \partial I_C)} \quad \ldots (5)$$

The above equation can be considered as a standard equation for derivation of stability factors of other biasing circuits.

STABILITY FACTOR (S) FOR FIXED BIAS CKT

$$I_B \equiv \frac{V_{CC}}{R_B}$$

When I_B changes by ∂I_B, V_{CC} and V_{BE} are unaffected.

$$\therefore \frac{\partial I_B}{\partial I_C} = 0 \quad \because I_C \text{ is not present in the equation.}$$

Substituting this value in equation (5), we get,

$$S = \frac{1+\beta}{1-\beta(\partial I_B / \partial I_C)} = \frac{1+\beta}{1-0}$$

$$S = 1+\beta \qquad \ldots (6)$$

STABILITY FACTOR (S^{I})

$$S' = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO},\beta \text{ constant}}$$

From equation (4) we have,

$$I_C = \beta I_B + (\beta + 1) I_{CBO}$$

Now representing I_B in terms of V_{BE} we get,

$$I_C = \beta \frac{(V_{CC} - V_{BE})}{R_B} + (\beta + 1) I_{CBO}$$

$$\therefore \quad I_C = \frac{\beta V_{CC}}{R_B} - \frac{\beta V_{BE}}{R_B} + (\beta + 1) I_{CBO} \quad \ldots (7)$$

$$\therefore \quad \frac{\partial I_C}{\partial V_{BE}} = 0 - \frac{\beta}{R_B} + 0 = \frac{-\beta}{R_B}$$

$$\therefore \quad S' = \frac{-\beta}{R_B} \quad \ldots (8)$$

RELATION B/W S & S^{I}

We know that $S = 1 + \beta$ and $S' = \frac{-\beta}{R_B}$

Multiplying numerator and denominator by $(1 + \beta)$ we have

$$S' = \frac{-\beta(1+\beta)}{R_B(1+\beta)}$$

$$S' = \frac{-\beta S}{R_B(1+\beta)} \qquad \because S = 1 + \beta \qquad \ldots (9)$$

STABILITY FACTOR (S^{II})

$$S'' = \left.\frac{\partial I_C}{\partial \beta}\right|_{V_{BE},\, I_{CO}\ \text{constant}}$$

From equation (7) we have

$$I_C = \frac{\beta V_{CC}}{R_B} - \frac{\beta V_{BE}}{R_B} + (\beta + 1)\, I_{CBO}$$

$$\therefore \quad \frac{\partial I_C}{\partial \beta} = \left(\frac{V_{CC}}{R_B} - \frac{V_{BE}}{R_B}\right) + I_{CBO} = I_B + I_{CBO} = \frac{I_C}{\beta}$$

$$\therefore \quad \frac{\partial I_C}{\partial \beta} = \frac{I_C}{\beta} \quad \text{Since } I_B = \frac{I_C}{\beta} \text{ and } I_B >> I_{CBO} \ \ldots (10)$$

RELATION B/W S & S^{II}

We know that $S = 1 + \beta$ and $S'' = \frac{I_C}{\beta}$

Multiplying numerator and denominator by $(1 + \beta)$ we have

$$S'' = \frac{I_C (1+\beta)}{\beta (1+\beta)}$$

$$\therefore \quad S'' = \frac{I_C\, S}{\beta\,(1+\beta)} \qquad \because \quad S = 1 + \beta \qquad \ldots (11)$$

VOLTAGE DIVIDER /SELF BIAS CIRCUIT

Voltage divider bias circuit

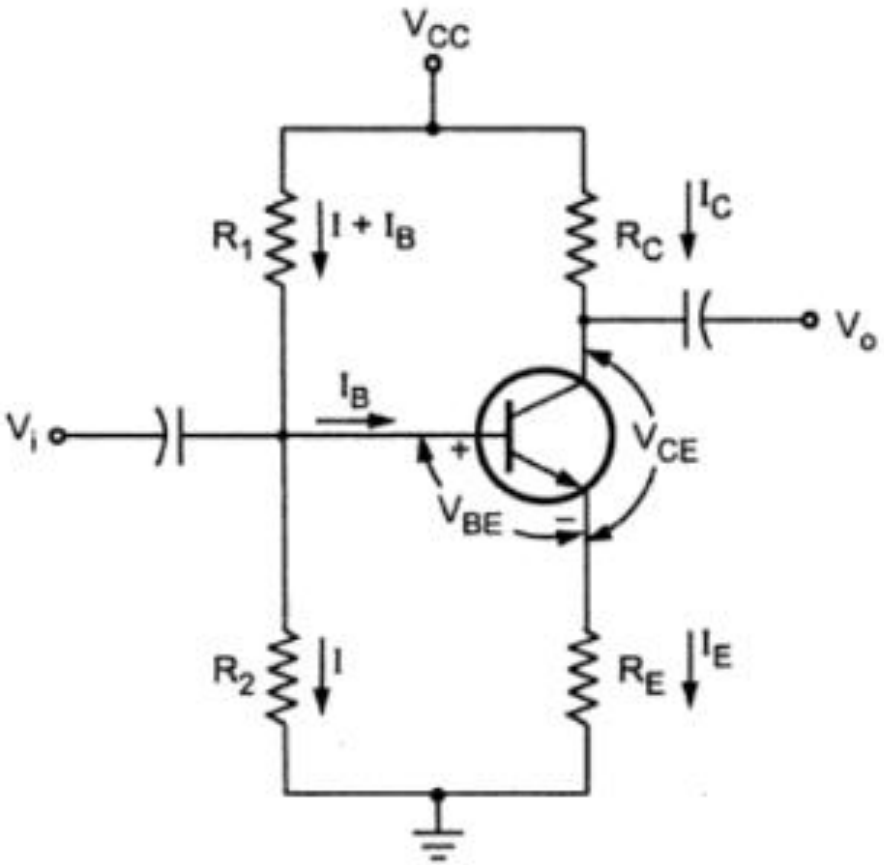
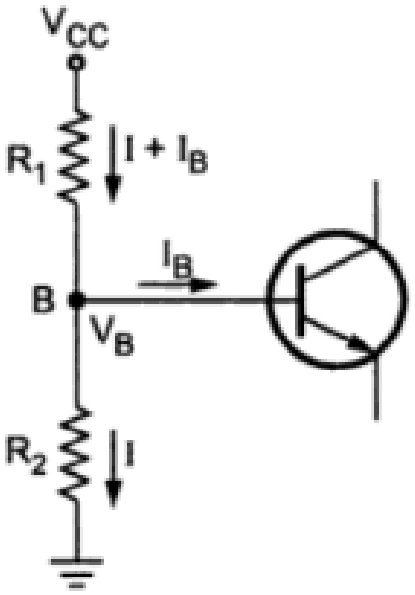


Fig. 1.29 shows the voltage divider bias circuit. In this circuit, the biasing is provided by three resistors : R_1, R_2 and R_E. The resistors R_1 and R_2 act as a potential divider giving a fixed voltage to point B which is base. If collector current increases due to change in temperature or change in β, the emitter current I_E also increases and the voltage drop across R_E increases, reducing the voltage difference between base and emitter (V_{BE}). Due to reduction in V_{BE}, base current I_B and hence collector current I_C also reduces. Therefore, we can say that negative feedback exists in the emitter bias circuit. This reduction in collector current I_C compensates for the original change in I_C.

Base circuit



Base circuit

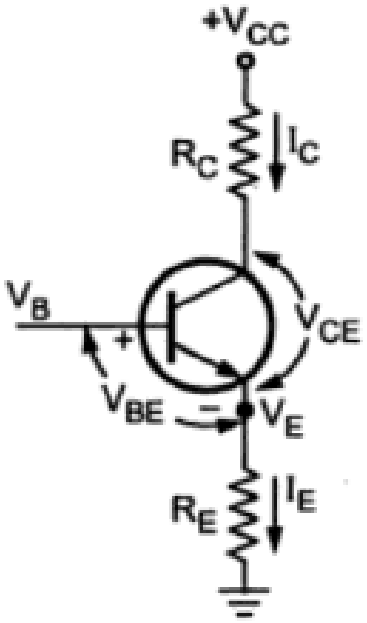
Let us consider the base circuit as shown in Fig. 1.30.

Voltage across R_2 is the base voltage V_B. Applying the voltage divider theorem to find V_B, we get,

$$V_B = \frac{R_2\,(I)}{R_1\,(I + I_B) + R_2\,(I)} \times V_{CC} \qquad \ldots (9)$$

$$V_B = \frac{R_2}{R_1 + R_2} \times V_{CC} \qquad \because\ I >> I_B \qquad \ldots (10)$$

Collector circuit



Now, let us consider the collector circuit as shown in Fig. 1.31.

Voltage across R_E (V_E) can be obtained as,

$$V_E = I_E R_E = V_B - V_{BE}$$

$$\therefore \quad I_E = \frac{V_B - V_{BE}}{R_E} \qquad \ldots (11)$$

Applying KVL to the collector circuit we get,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

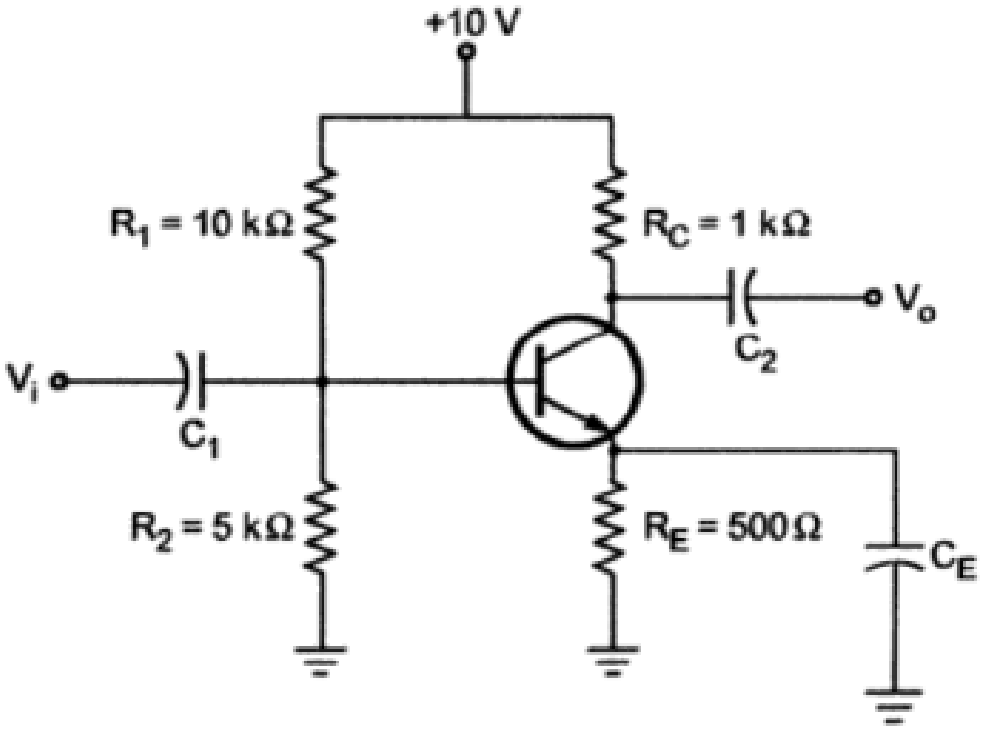
$$\therefore \quad V_{CE} = V_{CC} - I_C R_C - I_E R_E \qquad \ldots (12)$$

We can use simplified/approximate analysis when

$$\boxed{\beta R_E \geq 10 R_2}$$

Example 1.11 : *For the circuit shown in Fig. 1.33. $\beta = 100$ for the silicon transistor. Calculate V_{CE} and I_C.*

Figure 1.33



Solution : Since $\beta R_E = 50{,}000 = 10R_2$

We can use approximate analysis

$$V_B \cong \frac{R_2}{R_1 + R_2} V_{CC} = \frac{5 \times 10^3}{10 \times 10^3 + 5 \times 10^3} \times 10 = 3.33 \text{ V}$$

We know that, $V_E = V_B - V_{BE} = 3.33 - 0.7 = 2.63 \text{ V}$

and $I_E = \frac{V_E}{R_E} = \frac{2.63 \text{ V}}{500} = 5.26 \text{ mA}$

We know that, $I_B = \frac{I_E}{1 + \beta} = \frac{5.26 \times 10^{-3}}{101} = 52.08 \, \mu\text{A}$

and $I_C = \beta I_B = 100 \times 52.08 \times 10^{-6} = \mathbf{5.208 \text{ mA}}$

Applying KVL to the collector circuit we get,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

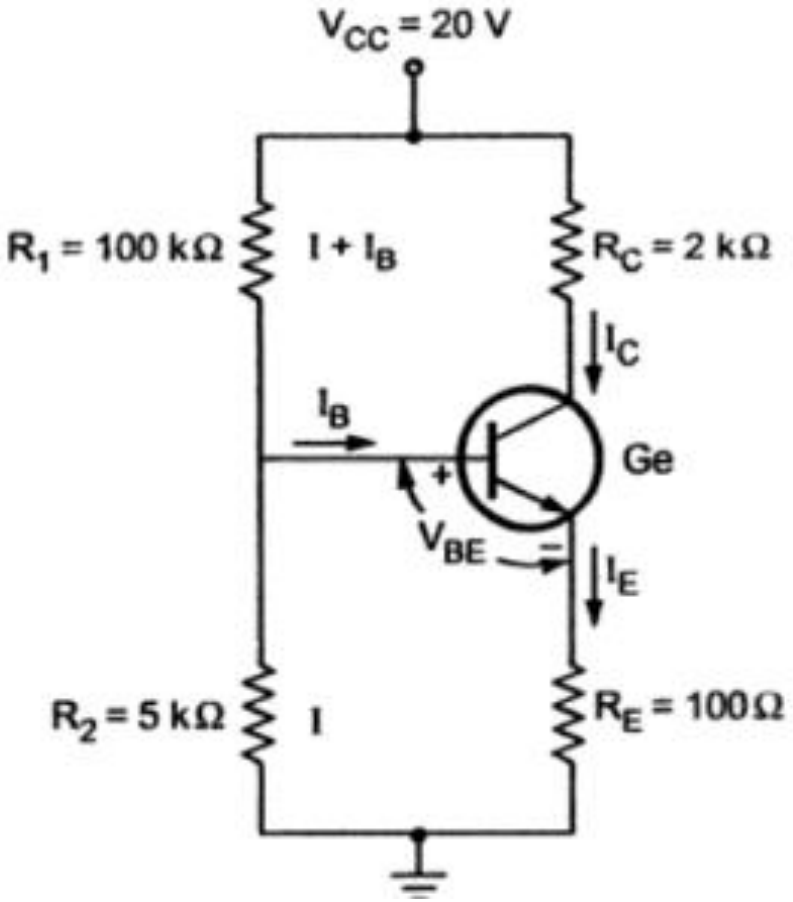
$$\therefore \quad V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$= 10 - 5.208 \times 10^{-3} \times 1 \times 10^3 - 5.26 \times 10^{-3} \times 500$$

$$= \mathbf{2.162 \text{ V}}$$

Example 1.12 : *For a circuit shown in Fig. 1.34,* $V_{CC} = 20\ V$, $R_C = 2\ k\Omega$, $\beta = 50$, $V_{BEact} = 0.2\ V$,
$R_1 = 100\ k\Omega$, $R_2 = 5\ k\Omega$ *and* $R_E = 100\ \Omega$. *Calculate* I_B, V_{CE} & I_C.

Figure 1.34



Solution : Since $\beta R_E = 5000 < 10\ R_2$ we have to use exact analysis.

$$V_{CC} = R_1 [I + I_B] + I R_2$$

$$\therefore \quad I = \frac{V_{CC} - I_B R_1}{R_1 + R_2}$$

$$V_{CC} = R_1 [I + I_B] + V_{BE} + I_E R_E$$

We know that, $I_E = I_B + I_C = I_B + \beta I_B$

$$\therefore \quad V_{CC} = R_1 [I + I_B] + V_{BE} + (1 + \beta) I_B R_E$$

Substituting value of I we get,

$$V_{CC} = R_1 \left[\frac{V_{CC} - I_B R_1}{R_1 + R_2} + I_B \right] + V_{BE} + (1 + \beta) I_B R_E$$

$$= R_1 \left[\frac{V_{CC} - I_B R_1 + I_B R_1 + I_B R_2}{R_1 + R_2} \right] + V_{BE} + (1 + \beta) I_B R_E$$

$$= R_1 \left[\frac{V_{CC} + I_B R_2}{R_1 + R_2} \right] + V_{BE} + (1 + \beta) I_B R_E$$

Substituting values of V_{CC}, R_1, R_2, V_{BE}, β and R_E

We get, $$20 = 100\times10^3\left[\frac{20+I_B\times5\times10^3}{100\times10^3+5\times10^3}\right]+0.2+(51)\,I_B\times100$$

$$20 = 19.047619 + 4761.9\,I_B + 0.2 + 5100\,I_B$$

$$0.752381 = 9861.9\,I_B$$

$$\therefore \quad I_B = \mathbf{76.29\ \mu A}$$

As $$I_C = \beta\, I_B = 50\times76.29\ \mu A = \mathbf{3.814\ mA}$$

Applying KVL to collector circuit we get,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$= I_C R_C + V_{CE} + (1+\beta) I_B R_E$$

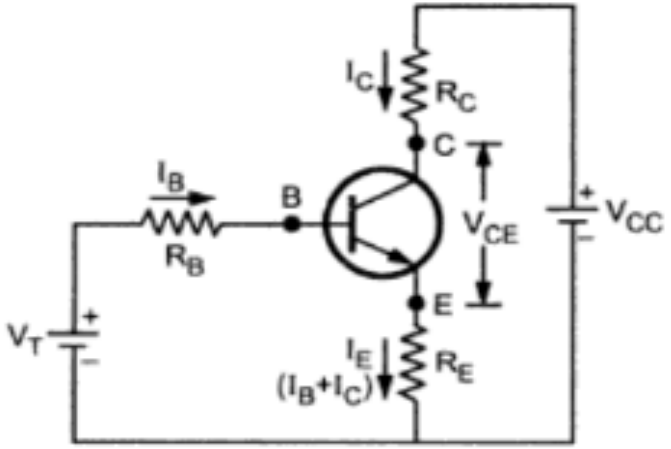
$$\therefore \quad V_{CE} = V_{CC} - I_C R_C - (1+\beta) I_B R_E$$

$$\therefore \quad V_{CE} = 20 - 3.814\times10^{-3}\times2\times10^3 - (51)\times76.29\times10^{-6}\times100$$

$$= \mathbf{11.983\ V}$$

STABILITY FACTOR (S)

Thevenin's equivalent circuit for voltage divider bias



For determining stability factor S for voltage divider bias we will consider the equivalent circuit as seen in the previous section. Fig. 1.38 shows the Thevenin's equivalent circuit for voltage divider bias.

Here Thevenin's equivalent voltage V_T is given by

$$V_T = \frac{R_2 \times V_{CC}}{R_1 + R_2} \quad \text{and}$$

the R_1 and R_2 are replaced by R_B which is the parallel combination of R_1 and R_2 .

$$\therefore \quad R_B = \frac{R_1 R_2}{R_1 + R_2}$$

Applying KVL to the base circuit we get,

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

Differentiating w.r.t. I_C and considering V_{BE} to be independent of I_C we get,

$$0 = \frac{\partial I_B}{\partial I_C} \times R_B + \frac{\partial I_B}{\partial I_C} \times R_E + R_E$$

$$\therefore \quad \frac{\partial I_B}{\partial I_C}(R_E + R_B) = -R_E$$

$$\therefore \quad \frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_E + R_B} \qquad \ldots (15)$$

We have already seen the generalized expression for stability factor S given by

$$S = \frac{1+\beta}{1-\beta\,(\partial I_B/\partial I_C)} \qquad \ldots (16)$$

Substituting value of $\frac{\partial I_B}{\partial I_C}$ in the equation (16) we get,

$$\mathbf{S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_E + R_B}\right)}} \qquad \ldots(17)$$

$$\Rightarrow \quad S = \frac{(1+\beta)(R_E + R_B)}{R_B + R_E + \beta R_E} = \frac{(1+\beta)(R_E + R_B)}{R_B + (1+\beta) R_E}$$

Key Point: *Stability factor S for voltage divider bias or self bias is less as compare to other biasing circuits studied. So this circuit is more stable and hence it is most commonly used. (Advantage of self bias or voltage divider bias circuit.)*

Advantages:

- Stability factor is less
- More stable

Disadvantage:

- Require more components than usual is the drawback of this method

STABILITY FACTOR(S^I)

Stability factor S′ is given by

$$S' = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO},\beta \text{ constant}}$$

It is the variation of I_C with V_{BE} when I_{CO} and β are considered constant.

We know that,

$$I_C = (1+\beta)\, I_{CO} + \beta\, I_B \qquad \ldots (20)$$

and

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

$\therefore$

$$V_{BE} = V_T - (R_E + R_B) I_B - R_E I_C \qquad \ldots (21)$$

By writing equation (20) in terms of I_B we get,

$$I_B = \frac{I_C - (1+\beta) I_{CO}}{\beta} \qquad \ldots (22)$$

Now, substituting I_B in equation (22) we get,

$$V_{BE} = V_T - (R_E + R_B)\left[\frac{I_C - (1+\beta)I_{CO}}{\beta}\right] - R_E I_C$$

$$= V_T - \frac{(R_E + R_B)I_C}{\beta} + \frac{(R_E + R_B)(1+\beta)I_{CO}}{\beta} - R_E I_C$$

$$\therefore \quad V_{BE} = V_T - \frac{[(1+\beta)R_E + R_B]I_C}{\beta} + \frac{(R_E + R_B)(1+\beta)I_{CO}}{\beta} \quad \ldots (23)$$

Differentiating the equation (23) w.r.t. V_{BE} with I_{CO} and β constant we get,

$$1 = 0 - \frac{[R_B + (1+\beta)R_E]}{\beta}\frac{\partial I_C}{\partial V_{BE}} + 0$$

$$\therefore \quad \frac{\partial I_C}{\partial V_{BE}} = \frac{-\beta}{R_B + (1+\beta)R_E} \quad \ldots (24)$$

$$\therefore \quad S' = \frac{-\beta}{R_B + (1+\beta)R_E} \quad \ldots (25)$$

RELATION B/W S & S'

We know from equation (17)

$$S = 1+\beta \frac{1+R_B/R_E}{1+\beta+R_B/R_E}$$

Multiplying both denominator and numerator by R_E we get,

$$S = \frac{(1+\beta)(R_E+R_B)}{R_B+(1+\beta)R_E} \quad \ldots (26)$$

$$\therefore \quad \frac{S}{(1+\beta)(R_E+R_B)} = \frac{1}{R_B+(1+\beta)R_E}$$

Substituting value of $\frac{1}{R_B+(1+\beta)R_E}$ in equation (25) we get,

$$S' = -\beta \frac{S}{(1+\beta)(R_E+R_B)} = -\frac{S}{(R_E+R_B)} \cdot \frac{\beta}{(1+\beta)} \quad \ldots (27)$$

STABILITY FACTOR(S^{II})

Stability factor S″ is given by

$$S'' = \left.\frac{\partial I_C}{\partial \beta}\right|_{I_{CO},\ V_{BE}\ \text{constant}}$$

It is the variation of I_C with β when I_{CO} and V_{BE} are considered constant. We recall equation (23) which is

$$V_{BE} = V_T - \frac{[R_B + (1+\beta)R_E]}{\beta} I_C + \left[\frac{(R_E + R_B)(1+\beta)}{\beta}\right] I_{CO}$$

$$= V_T - \frac{[R_B + (1+\beta)R_E]}{\beta} I_C + V' \qquad \ldots (28)$$

where $$V' = \left[\frac{(R_B + R_E)(\beta+1)}{\beta}\right] I_{CO} = (R_B + R_E) I_{CO} \qquad \because \ \beta >> 1$$

If we write equation (28) in terms of I_C we get,

$$I_C = \frac{\beta(V_T + V' - V_{BE})}{R_B + R_E(1+\beta)} \qquad \ldots (29)$$

Differentiating equation 29 and taking V′ independent of β , we get,

$$\frac{\partial I_C}{\partial \beta} = \frac{R_B + R_E (1+\beta)(V_T + V' - V_{BE}) - \beta (V_T + V' - V_{BE}) R_E}{(R_B + R_E (1+\beta)^2)}$$

$$\left[\text{Hint: } \frac{d}{dt}\left(\frac{u}{v}\right) = \frac{v \times \frac{du}{dt} - u \times \frac{dv}{dt}}{v^2} \right]$$

Multiplying numerator and denominator by $(1 + \beta)$ we get,

$$= \frac{(1+\beta)(R_B + R_E)(V_T + V' - V_{BE})}{(1+\beta)[R_B + R_E (1+\beta)][R_B + R_E (1+\beta)]}$$

$$= \frac{S(V_T + V' - V_{BE})}{(1+\beta)[R_B + R_E (1+\beta)]}$$

Since $S = \frac{(1+\beta)(R_E + R_B)}{R_B + (1+\beta) R_E}$ from equation (26)

Multiplying numerator and denominator by β we get,

$$\frac{\partial I_C}{\partial \beta} = \frac{\beta (V_T + V' - V_{BE}) S}{\beta (1+\beta) [R_B + R_E (1+\beta)]} = \frac{I_C S}{\beta (1+\beta)} \quad \ldots (30)$$

Since $$I_C = \frac{\beta (V_T + V' - V_{BE})}{[R_B + R_E (1+\beta)]}$$

$\therefore$ $$S'' = \frac{\partial I_C}{\partial \beta} = \frac{I_C S}{\beta (1+\beta)} \quad \ldots (31)$$

Thus, change in collector current due to change in β is

$$\partial I_C = S'' \partial \beta = \frac{I_C S}{\beta (1+\beta)} \partial \beta$$

Small signal analysis of amplifiers

By
sudheer

BASIC TRANSISTOR AMPLIFIER

The Fig. 6.13 shows basic amplifier circuit. From the Fig. 6.13 we can notice that to form a transistor amplifier only it is necessary to connect an external load and signal source, along with proper biasing. Fig. 6.13 represents a transistor in any one of the three possible configurations.

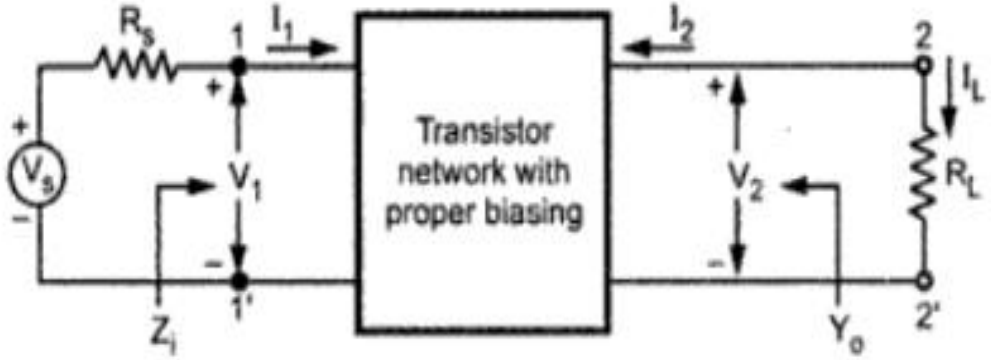


Fig. 6.13 Basic transistor amplifier

We can replace transistor circuit shown in Fig. 6.13 with its small signal hybrid model

H-parameters or hybrid parameters

- h parameter of two port network is a square matrix of order 2×2. Basically it is a way to represent a two port network. It is also known as hybrid parameter. In this form of representation, voltage of input port and current of the output port is expressed in terms of current of input port and voltage of output port.
- Thus, the h parameter for a two port network is defined as

$$\begin{bmatrix} V1 \\ I2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I1 \\ V2 \end{bmatrix} \quad \text{.....(1)}$$

$$\Rightarrow V_1 = h_{11}I_1 + h_{12}V_2 \text{.....(2)}$$

$$\Rightarrow I_2 = h_{21}I_1 + h_{22}V_2 \text{.....(3)}$$

Why h Parameter is called Hybrid Parameter?

- h parameter is also called hybrid parameter. This is because of the method of calculation of individual element of h matrix. Short circuit condition of input port is assumed for the calculation of h_{11} and h_{21}.
- While open circuit condition is assumed for h_{12} and h_{22} calculation. Thus we see that, both open circuit and short circuit terminal conditions are assumed in the calculation of h_{11}, h_{12}, h_{21} and h_{22}. This is the reason, it is also called hybrid parameter.

Calculation of h Parameter:

- Let us consider a two port network. Let V_1, I_1, V_2 and I_2 are the input voltage, input current, output voltage and output current respectively.

- Assuming the short circuit condition at the output terminal, we get

$$V_2 = 0$$

- Now putting $V_2 = 0$ in (2), we get

$$V_1 = h_{11} I_1$$

$$\boldsymbol{h_{11} = (V_1 / I_1)}$$

- Similarly putting $V_2 = 0$ in (3), we get

$$I_2 = h_{21} I_1$$

$$\boldsymbol{h_{21} = (I_2 / I_1)}$$

- Again assuming input port of the two port network to be open circuited, the input voltage will be zero.

$$I_1 = 0$$

- Now putting $I_1 = 0$ in (2), we get

$$V_1 = h_{12}V_2$$

$$\boldsymbol{h_{12} = (V_1 / V_2)}$$

- Similarly putting $I_1 = 0$ in (3), we get

$$I_2 = h_{22}V_2$$

$$\boldsymbol{h_{22} = (I_2 / V_2)}$$

H parameters of two port network

h_{11}	(V_1 / I_1)	Condition: Output port of the two port network is short circuited i.e. $V_2 = 0$
h_{21}	(I_2 / I_1)	
h_{12}	(V_1 / V_2)	Condition: Input port of the two port network is open circuited i.e. $I_1 = 0$
h_{22}	(I_2 / V_2)	

- Since h_{11} is the ratio of input voltage and input current when the output port is short circuited, therefore it is known ***Input Impedance***. Its unit is ohm.
- h_{22} is the ratio of output current and output voltage when input port is open circuited, therefore it is called ***Output Admittance*** of the network. Its unit is mho.
- h_{12} is the ratio of input voltage and output voltage when input port is open circuited, therefore it is called ***Reverse Voltage Gain***. It is a unit less quantity.
- h_{21} is the ratio of output current and input current when output port is short circuited, therefore it is called ***Forward Current Gain***. It is a unit less quantity.

Equivalent Circuit Representation of h Parameter:

We can replace transistor circuit shown in Fig. 6.13 with its small signal hybrid model as shown in Fig. 6.14.

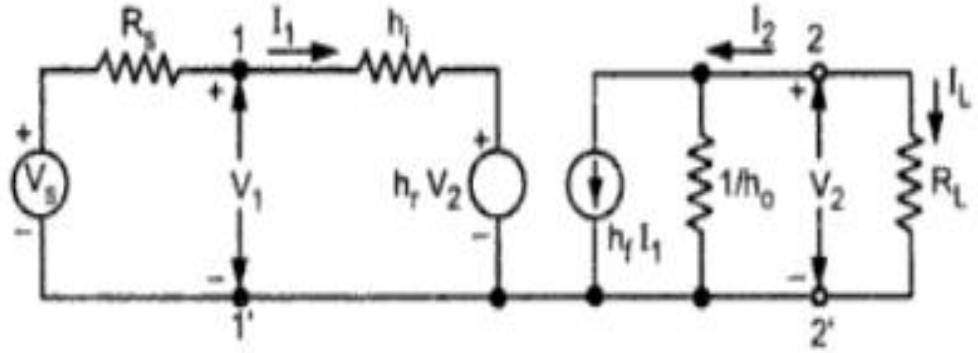


Fig. 6.14 Transistor amplifier in its h-parameter model

Let us analyze hybrid model to find the current gain, the input resistance, the voltage gain, and the output resistance.

Current gain(A_i)

Current Gain (A_i) :

For transistor amplifier A_i is defined as the ratio of output to input currents. It is given by,

$$A_i = \frac{I_L}{I_1} = -\frac{I_2}{I_1} \quad \ldots (1)$$

Here I_L and I_2 are equal in magnitude but opposite in sign, i.e. $I_L = -I_2$

From the circuit of Fig. 6.14 We have,

$$I_2 = h_f I_1 + h_o V_2 \quad \ldots (2)$$

Substituting $V_2 = -I_2 R_L$ in the equation we obtain

$$I_2 = h_f I_1 + h_o (-I_2 R_L)$$

$$\therefore \quad I_2 + h_o I_2 R_L = h_f I_1$$

$$\therefore \quad (1 + h_o R_L) I_2 = h_f I_1$$

$$\frac{I_2}{I_1} = \frac{h_f}{1 + h_o R_L}$$

$$\boxed{A_i = -\frac{I_2}{I_1} = \frac{-h_f}{1 + h_o R_L}}$$

Current gain(A_{is})

It is the current gain taking into account the source resistance, R_S if the model is driven by the current source instead of voltage source. It is given by

$$A_{is} = -\frac{I_2}{I_s} = -\frac{I_2}{I_1} \cdot \frac{I_1}{I_s} \quad \ldots (4)$$

$$= A_i \cdot \frac{I_1}{I_s}$$

(a) Input section of hybrid model current source

(b) Input section of hybrid model with instead of voltage source

Fig. 6.15

Looking at Fig. 6.15 (b) and using current divider equation we get

$$I_1 = \frac{I_s R_s}{Z_i + R_s}$$

$$\therefore \quad \frac{I_1}{I_s} = \frac{R_s}{Z_i + R_s}$$

And hence $$A_{is} = \frac{A_i R_s}{Z_i + R_s} \quad \ldots (5)$$

Input impedance (Z_i)

As shown in the Fig. 6.13, R_i is 'he input resistance looking into the amplifier input terminals (1, 1′). It is given by,

$$R_i = \frac{V_1}{I_1} \quad \ldots (6)$$

From the input circuit of Fig. 6.14, we have

$$V_1 = h_i I_1 + h_r V_2 \quad \ldots (7)$$

Hence $$Z_i = \frac{V_1}{I_1} = \frac{h_i I_1 + h_r V_2}{I_1}$$

$$\therefore \quad Z_i = h_i + h_r \frac{V_2}{I_1} \quad \ldots (8)$$

Substituting $$V_2 = -I_2 R_L = A_i I_1 R_L \quad \ldots (9)$$

In the above equation we get,

$$Z_i = h_i + \frac{h_r A_i I_1 R_L}{I_1} = h_i + h_r A_i R_L \quad \ldots (10)$$

Substituting $$A_i = -\frac{n_f}{1 + h_o R_L}$$

We get, $$Z_i = h_i - \frac{h_r h_f R_L}{1 + h_o R_L} \quad \ldots (11)$$

Dividing numerator and denominator by R_L we get

$$Z_i = h_i - \frac{h_r h_f}{1/R_L + h_o}$$

$\therefore$ $$\boxed{Z_i = h_i - \frac{h_r h_f}{Y_L + h_o}} \quad \text{where } Y_L = \frac{1}{R_L} \quad \ldots (12)$$

From this equation we can note that input impedance is a function of the load impedance.

Voltage Gain(A_V)

It is the ratio of output voltage V_2 to the input voltage V_1 . It is given by

$$A_v = \frac{V_2}{V_1} \quad \ldots (13)$$

From equation (9) we have,

$$\therefore \quad \boxed{A_v = \frac{A_i \, I_1 \, R_L}{V_1} = \frac{A_i \, R_L}{Z_i}} \quad \ldots (14)$$

Since, $\frac{I_1}{V_1} = \frac{1}{Z_i}$

Voltage Gain(A_{VS})

Voltage Gain (A_{vs}) : It is voltage gain including the source. It is given by,

$$A_{vs} = \frac{V_2}{V_S} = \frac{V_2}{V_1} \times \frac{V_1}{V_S} \quad \ldots (15)$$

$$\therefore \quad A_{vs} = A_v \times \frac{V_1}{V_S} \quad \ldots (16)$$

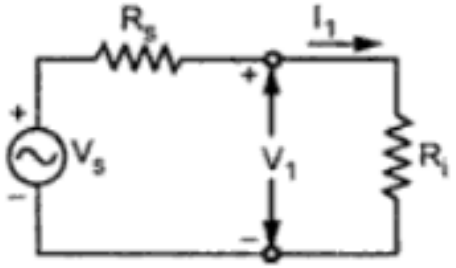


Fig. 6.16

Looking at Fig. 6.16 and applying potential divider theorem we can write,

$$V_1 = \frac{Z_i}{R_s + Z_i} V_S$$

$$\therefore \quad \frac{V_1}{V_S} = \frac{Z_i}{R_s + Z_i}$$

Substituting value of $\frac{V_1}{V_S}$ in equation 16 We get,

$$\therefore \quad \boxed{A_{vs} = A_v \cdot \frac{Z_i}{R_s + Z_i}} \quad \ldots (17)$$

$$= \frac{A_i R_L}{R_s + R_i} \quad \because A_v = \frac{A_i R_L}{Z_i} \quad \ldots (18)$$

Output admittance(Y_0)

It is the ratio of output current I_2 to the output voltage V_2. It is given by,

$$Y_o = \frac{I_2}{V_2} \text{ with } V_s = 0 \quad \ldots (19)$$

From equation (2), we have, $I_2 = h_f I_1 + h_o V_2$

Dividing above equation by V_2 we get,

$$\frac{I_2}{V_2} = \frac{h_f I_1}{V_2} + h_o$$

$$\therefore \quad Y_o = h_f \frac{I_1}{V_2} + h_o \quad \ldots (20)$$

From Fig. 6.14, with $V_s = 0$ we can write,

$$R_s I_1 + h_i I_1 + h_r V_2 = 0 \quad \ldots (21)$$

$$\therefore \quad (R_s + h_i) I_1 = -h_r V_2$$

$$\therefore \quad \frac{I_1}{V_2} = \frac{-h_r}{R_s + h_i} \qquad \ldots (22)$$

Substituting value of $\frac{I_1}{V_2}$ from equation (22) in equation (20), we obtain,

$$\therefore \quad \boxed{Y_o = h_o - \frac{h_f\, h_r}{h_i + R_s}} \qquad \ldots (23)$$

From this equation we can note that output admittance is a function of the source resistance.

Power Gain(A_p)

Power Gain (A_P) : It is the ratio of average power delivered to the load R_L, to the input power. Output power is given as

$$P_2 = V_2 I_L = -V_2 I_2 \quad \ldots (24)$$

Since the input power is $P_1 = V_1 I_1$ the operating power gain A_P of the transistor is defined as

$$\therefore \quad \boxed{A_P = \frac{P_2}{P_1} = -\frac{V_2 I_2}{V_1 I_1} = A_v A_i = A_i^2 \frac{R_L}{Z_i}} \quad \because A_v = \frac{A_i R_L}{Z_i} \quad \ldots (25)$$

Relation between A_{VS} & A_{IS}

From equations(18) and equation(5) we have

$$A_{vs} = \frac{A_i \, R_L}{Z_i + R_s}$$

and

$$A_{is} = \frac{A_i \, R_s}{Z_i + R_s}$$

Taking ratio of above two equations we get,

$$\frac{A_{vs}}{A_{is}} = \frac{R_L}{R_s}$$

$$\therefore \quad \boxed{A_{vs} = A_{is} \cdot \frac{R_L}{R_s}} \qquad \ldots (26)$$

$A_i = -\dfrac{h_f}{1+h_o R_L}$
$A_{is} = \dfrac{A_i R_s}{Z_i + R_s}$
$Z_i = h_i + h_r A_i R_L = h_i - \dfrac{h_f h_r}{h_o + Y_L}$
$A_v = \dfrac{A_i R_L}{Z_i}$
$A_{VS} = \dfrac{A_v R_i}{Z_i + R_s} = \dfrac{A_i R_L}{Z_i + R_s} = \dfrac{A_{is} R_L}{R_s}$
$Y_o = h_o - \dfrac{h_f h_r}{h_i + R_s} = \dfrac{1}{Z_o}$
$A_P = A_V A_i = A_i^2 \dfrac{R_L}{Z_i}$

GUIDELINES FOR ANALYSIS OF TRANSISTOR CIRCUIT

In the previous section we have seen generalized transistor circuit analysis using h-parameters. There are many transistor circuits. Circuits may consist of different biasing techniques, different configurations and so on. The analysis of such transistor circuits for its small signal behaviour can be made by following simple guidelines. These guidelines are :

1. Draw the actual circuit diagram.
2. Replace coupling capacitors and emitter bypass capacitor by short circuit.
3. Replace d.c. source by a short circuit. In other words, short V_{CC} and ground lines.
4. Mark the points B(base), C(collector), E(emitter) on the circuit diagram and locate these points as the start of the equivalent circuit.
5. Replace the transistor by its h-parameter model.

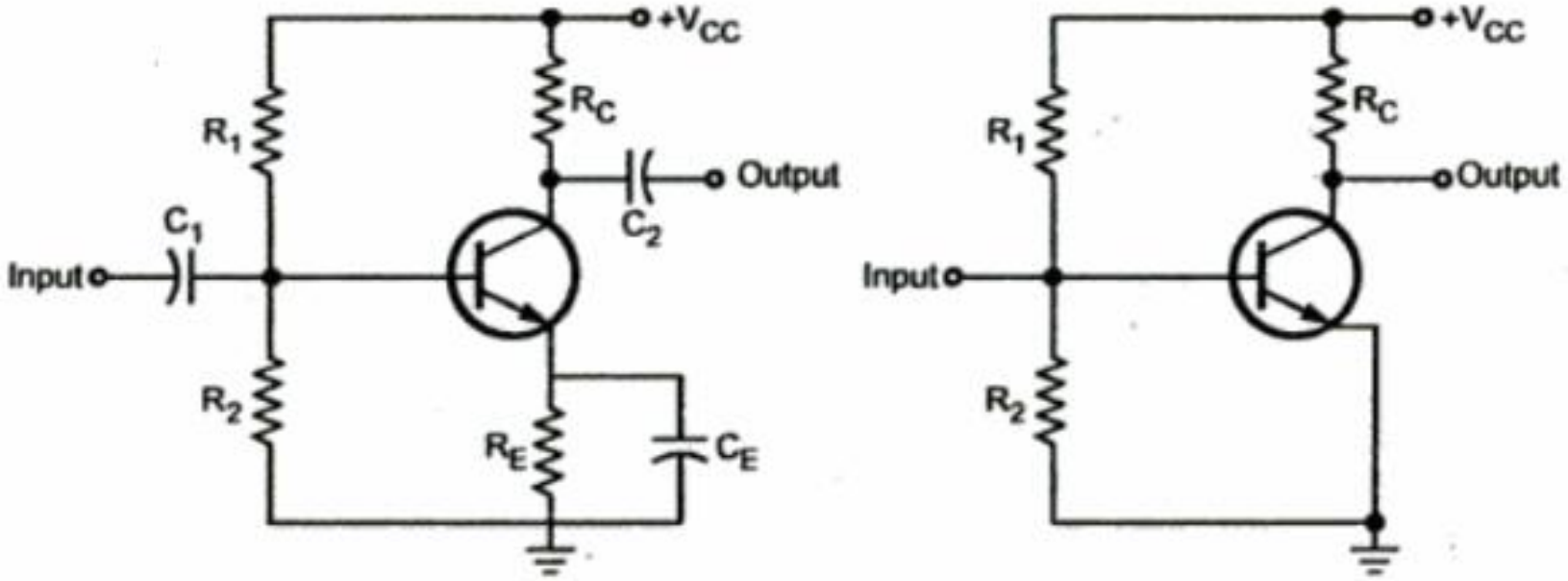
Consider a common emitter amplifier with voltage divider bias circuit as shown in the Fig. 6.17 (a)

Guideline 1 : Draw actual circuit diagram

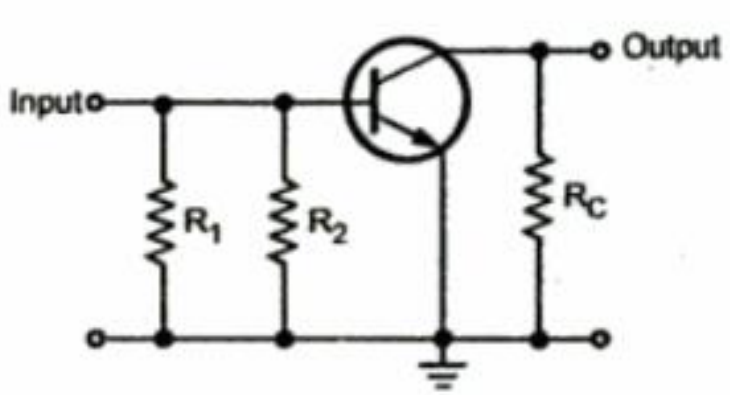
Guideline 2 : Short coupling and bypass capacitors

Guideline 3 : Short V_{CC} and ground lines

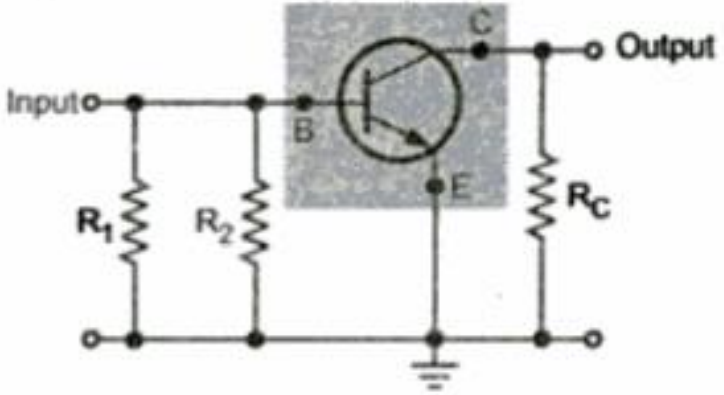
Guideline 4 : Mark points B, C, E and locate these points as the start of the equivalent circuit



(a) Actual circuit diagram **(b) Circuit with capacitors as a short circuit**



(c) Circuit with V_{CC} and ground short circuit



(d) Circuit with B, C and E points located

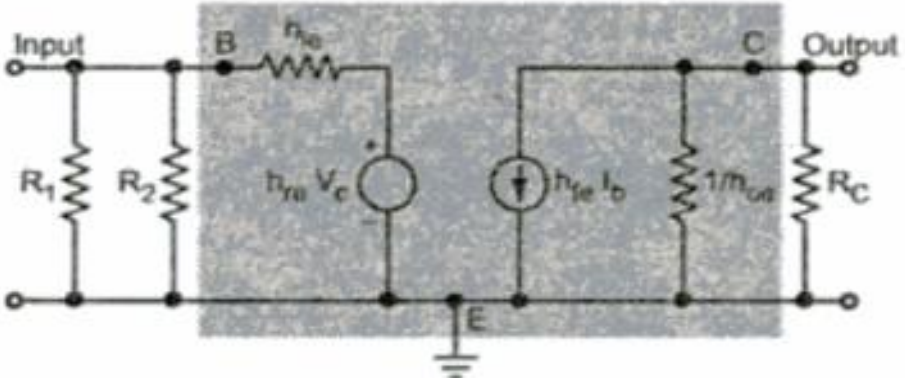
Fig. 6.17

Guideline 5 : Replace transistor by its h-parameter model and calculate effective R_i (R_i') and effective R_o (R_o').

For example, in above circuit $R_i' = R_1 \parallel R_2 \parallel R_i$

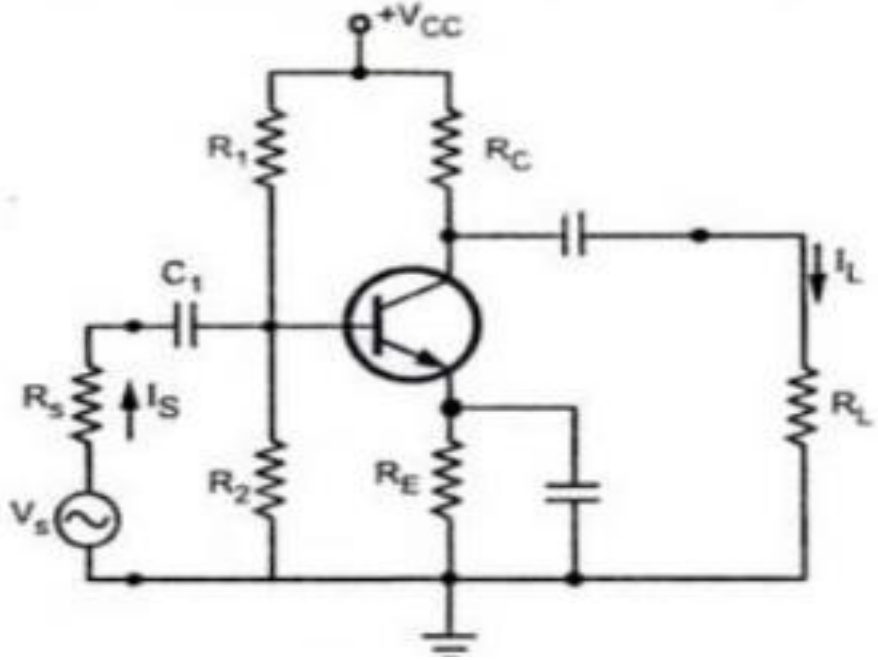
and $R_o' = R_o \parallel R_C$.

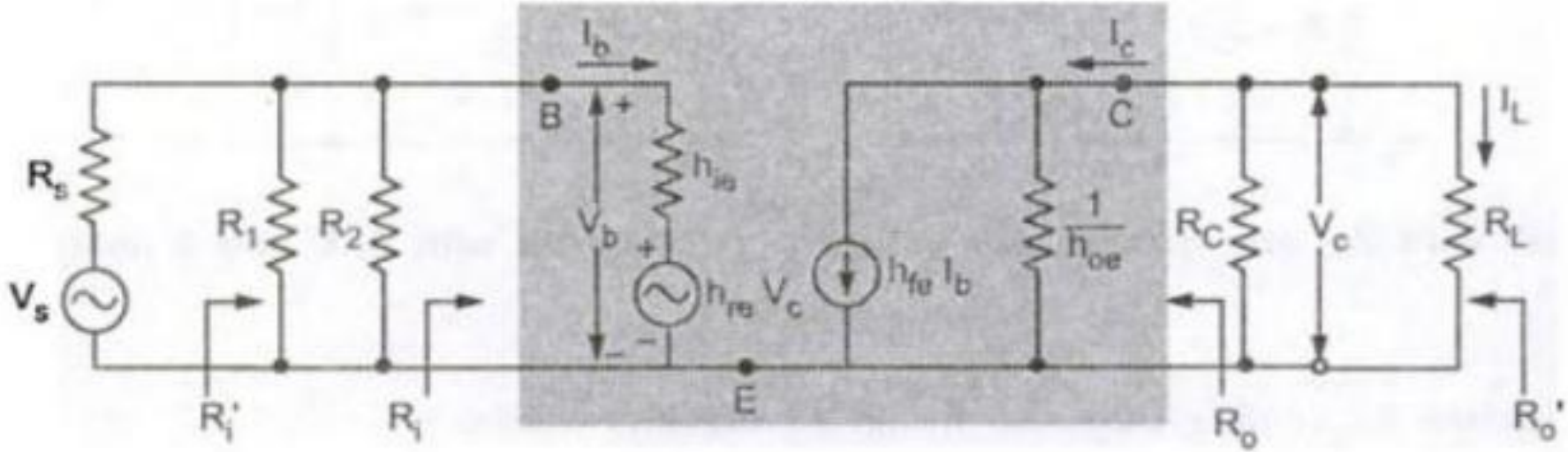
With these guidelines we will analyze CE,CB and CC amplifier circuits in coming sections.



Example 6.1 : *Consider a single stage CE amplifier with* $R_s = 1\ k\Omega$, $R_1 = 50\ K$, $R_2 = 2\ K$, $R_C = 1\ K$, $R_L = 1.2\ K$, $h_{fe} = 50$, $h_{ie} = 1.1\ K$, $h_{oe} = 25\ \mu A/V$ *and* $h_{re} = 2.5 \times 10^{-4}$, *as shown in Fig. 6.18.*

Find A_v, R_i, A_{vs}, $A_i = \frac{I_L}{I_S}$, $A_{VS} = \frac{V_0}{V_s}$ *and* R_o.





a) Current gain $A_i = \dfrac{-I_c}{I_b} = \dfrac{-h_{fe}}{1+h_{oe}R'_L}$

Where $R'_L = R_C \parallel R_L = 1\ K \parallel 1.2\ K = \mathbf{545.45\ \Omega}$

$\therefore$ $A_i = \dfrac{-50}{1+25\,\mu A/V(545.45)} = \mathbf{-49.32}$

b) Input resistance $R_i = h_{ie} + h_{re}\,A_i\,R'_L$

$= 1.1\ K + 2.5\times10^{-4}\times(-49.32)\times545.45$

$= \mathbf{1093\ \Omega}$

c) Voltage gain $A_v = \dfrac{V_c}{V_b} = \dfrac{A_i\,R'_L}{R_i} = \dfrac{-49\,32\times545.45}{1093} = \mathbf{-24.61}$

d) Overall input resistance $R'_i = R_i \parallel R_1 \parallel R_2 = 1093 \parallel 50\ K \parallel 2\ K = \mathbf{696.9\ \Omega}$

e) Overall voltage gain $A_{vs} = \dfrac{V_c}{V_s} = \dfrac{V_c}{V_b}\times\dfrac{V_b}{V_s}$

Looking at Fig. 6.20 and voltage divider equation we get,

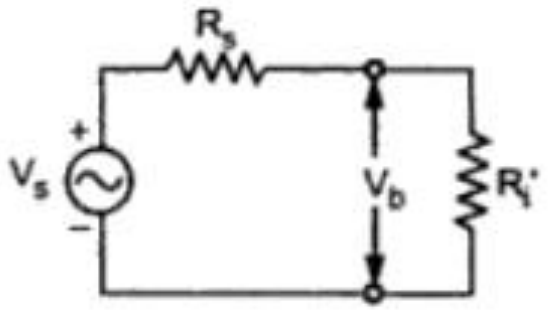


Fig. 6.20

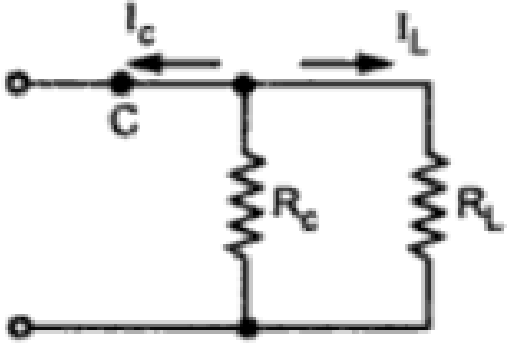
$$V_b = \frac{V_s\, R_i'}{R_s + R_i'} \quad \therefore \quad \frac{V_b}{V_s} = \frac{R_i'}{R_s + R_i'}$$

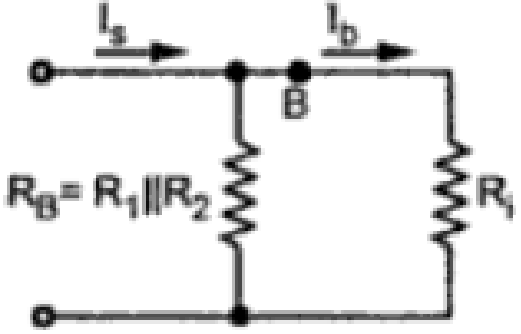
$$\therefore \quad A_{vs} = \frac{V_c}{V_b} \times \frac{V_b}{V_s} = A_v \times \frac{R_i'}{R_s + R_i'}$$

$$= 24.61 \times \frac{696.9}{1\text{ k} + 696.9} = \mathbf{10.1}$$

f) $$A_{i(\text{for circuit})} = \frac{I_L}{I_s} = \frac{I_L}{I_c} \times \frac{I_c}{I_b} \times \frac{I_b}{I_s}$$

Looking at Fig. 6.21 and 6.22 and using current divider equation we have,





$$I_L = \frac{-I_c R_C}{R_C + R_L}$$

$$\therefore \quad \frac{I_L}{I_c} = \frac{-R_C}{R_C + R_L}$$

and $$I_b = \frac{I_s R_B}{R_B + R_i}$$

Where $R_B = R_1 \parallel R_2 = 50\ K \parallel 2\ K = 1.923\ K$

$$\therefore \quad \frac{I_b}{I_s} = \frac{R_B}{R_B + R_i}$$

$$\therefore \quad A_{i\ (\text{for circuit})} = \frac{I_L}{I_c} \times \frac{I_c}{I_b} \times \frac{I_b}{I_s} = \frac{-R_C}{R_C + R_L} \times 49.32 \times \frac{R_B}{R_B + R_i}$$

$$= \frac{-1\ K}{1K + 1.2\ K} \times 49.32 \times \frac{1.923\ K}{1.923\ K + 1.093\ K} = \mathbf{-14.29}$$

ANALYSIS OF CE CIRCUIT USING SIMPLIFIED HYBRID MODEL

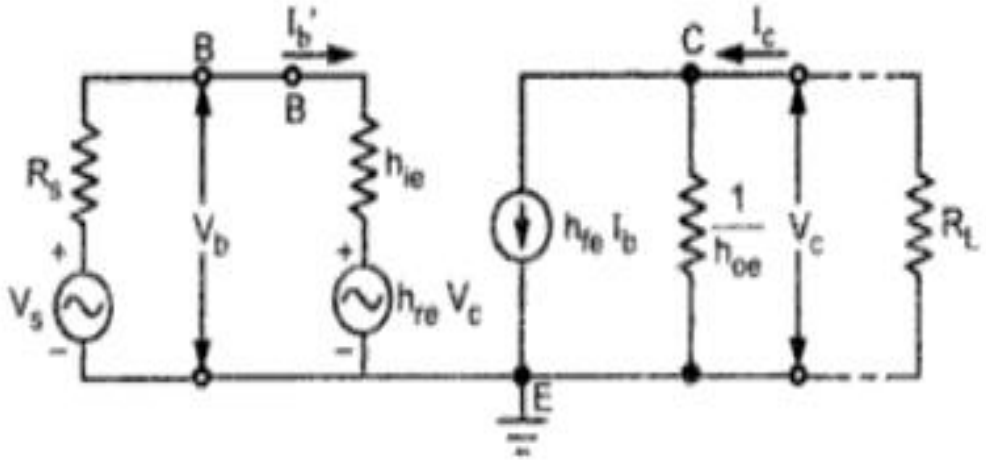


Fig. 6.31

Let us consider the h-parameter equivalent circuit for the amplifier, as shown in the Fig. 6.31.

Now, see how can we modify this model so as to make the analysis simple without greatly sacrificing accuracy ?

Since $1/h_{oe}$ is in parallel with R_L and R_C if $1/h_{oe} >> R_L \parallel R_C$, then h_{oe} may be neglected. If we neglect h_{oe}, the collector current I_c is given by $I_c = h_{fe} I_b$. Under these conditions the magnitude of the voltage of the generator in the emitter circuit is,

$$h_{re} |V_{ce}| = h_{re} I_c (R_L \parallel R_C) = h_{re} h_{fe} I_b (R_L \parallel R_C)$$

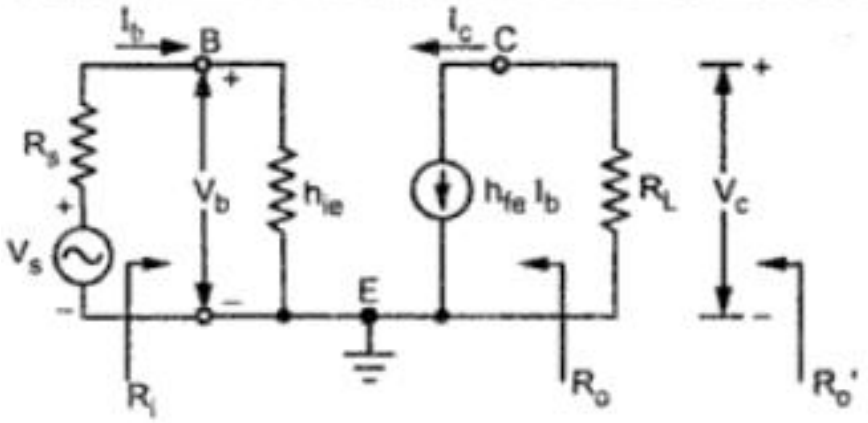


Fig. 6.32 Approximate CE model

Since $h_{re}h_{fe} \approx 0.01$, this voltage may be neglected in comparison with the $h_{ie}I_b$ drop across h_{ie}, provided that $R_L \parallel R_C$ is not too large. We therefore conclude that if the load resistance $R_L \parallel R_C$ is small, it is possible to neglect the parameters h_{re} and h_{oe} in the h-parameter equivalent circuit. Fig. 6.32 shows the approximate h-parameter equivalent circuit.

Current Gain : From Table 6.2 the CE current gain is given as

$$A_i = \frac{-I_c}{I_b} = \frac{-h_{fe}}{1+h_{oe}R_L}$$

By neglecting h_{oe} we have, $A_i \approx -h_{fe}$ ...(1)

Input Impedance : From Table 6.2 the CE input impedance is given as

$$R_i = h_{ie} + h_{re} A_i R_L$$

By neglecting h_{re} we have,

$$R_i \approx h_{ie} \quad ...(2)$$

Voltage Gain : From Table 6.2 the voltage gain is given as

$$\boxed{A_v = \frac{A_i R_L}{R_i} = \frac{A_i R_L}{h_{ie}}} \quad \ldots(3)$$

Output Impedance : From Table 6.2 the CE output impedance is given as

$$\boxed{Y_o = h_{oe} - \frac{h_{fe} h_{re}}{h_{ie} + R_s}} \quad \ldots(3)$$

By neglecting h_{oe} and h_{re}

$$Y_o = 0$$

$$\therefore \quad R_o = \frac{1}{Y_o} = \infty \quad \ldots(4)$$

$$\boxed{R'_o = R_o \parallel R_L = \infty \parallel R_L = R_L} \quad \ldots(5)$$

ANALYSIS OF CC CIRCUIT USING SIMPLIFIED HYBRID MODEL

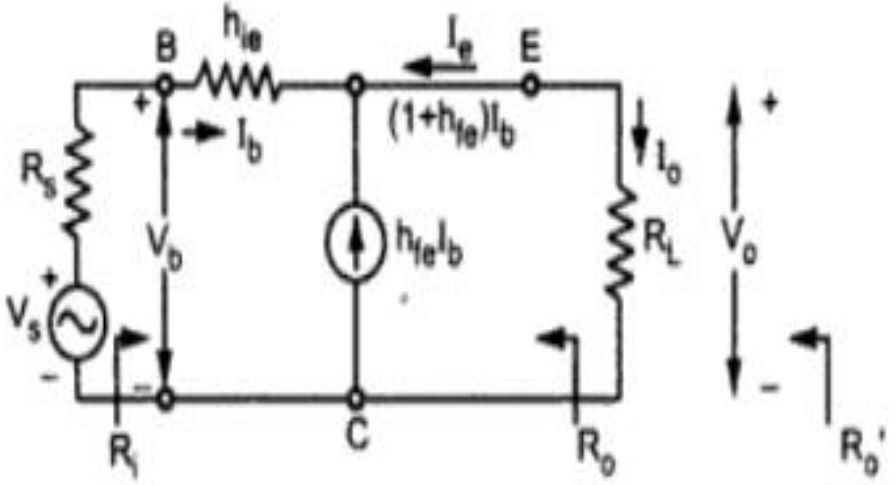


Fig. 6.37 Simplified CC model

We have seen the simplified CE model, in which input is applied to base and output is taken from collector, and emitter is common between input and output. The same simplified model can be modified to get simplified CC model. For simplified CC model, we have to make collector common and take the output from emitter, as shown in the Fig. 6.37. The h_{fe} I_b current direction is now exactly opposite that of CE model because the current h_{fe} I_b always points towards emitter.

Current Gain : It is defined as the ratio of output to input currents

$$\boxed{A_i = \frac{I_o}{I_b} = \frac{-I_e}{I_b} = 1 + h_{fe}} \quad \ldots (6)$$

Input Resistance :

From Fig. 6.37 we obtain $R_i = \frac{V_b}{I_b}$

Applying KVL we have

$$V_b - I_b h_{ie} - I_o R_L = 0$$

$$\therefore \quad V_b = I_b h_{ie} + I_o R_L$$

$$\therefore \quad \frac{V_b}{I_b} = h_{ie} + \frac{I_o}{I_b} R_L$$

$$\boxed{R_i = \frac{V_b}{I_b} = h_{ie} + (1 + h_{fe}) R_L} \quad \because \quad \frac{I_o}{I_b} = \frac{-I_e}{I_b} = 1 + h_{fe} \quad \ldots (7)$$

The above equation shows that input impedance of CC is higher than the CE configuration.

Voltage Gain (A_v) :

It is given as $A_V = \frac{V_o}{V_b} = \frac{I_o R_L}{I_b R_i} = \frac{A_i R_L}{R_i} \because A_i = \frac{I_o}{I_b} = \frac{-I_e}{I_b}$ ...(8)

Substituting values of A_i and R_i we get

$$\boxed{A_v = \frac{(1+h_{fe})R_L}{h_{ie}+(1+h_{fe})R_L} \cong 1}$$ but always less than 1 $\because$ $(1 + h_{fe}) R_L >> h_{ie}$ ...(9)

Output Resistance R_o :

It is the ratio of output voltage V_o to output current I_e with $V_s = 0$

$$R_o = \left.\frac{V_o}{I_e}\right|_{V_s=0}$$

Applying KVL we have,

$V_s - I_b R_s - I_b h_{ie} - V_o = 0$

$\therefore$ $V_o = - I_b R_s - I_b h_{ie}$ $\because$ $V_s = 0 = - I_b (R_s + h_{ie})$

$I_e = - (1 + h_{fe}) I_b$

$\therefore$ $\frac{V_o}{I_e} = \frac{-I_b(R_s+h_{ie})}{-(1+h_{fe})I_b}$

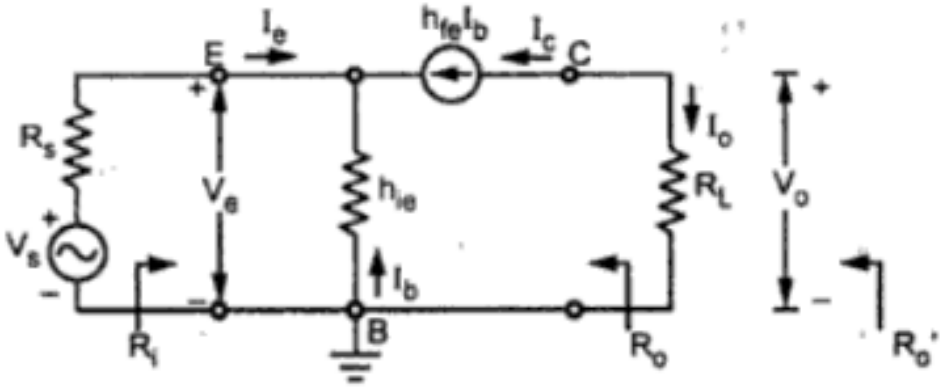
$$\therefore \quad \boxed{R_o = \frac{V_o}{I_e} = \frac{R_s + h_{ie}}{1 + h_{fe}}} \qquad \ldots (10)$$

The output resistance R'_o of the stage, taking the load into account is given as

$$\therefore \quad \boxed{R'_o = R_o \parallel R_L} \qquad \ldots (11)$$

6.6.3 Analysis of Common Base Circuit using Simplified Model

The approximate CB model can be drawn by giving input to emitter, taking output from collector and making base common. The Fig. 6.41 shows the approximate CB model.



Current Gain (A_i) : It is defined as a ratio of output to input currents

$$\therefore \quad A_i = \frac{I_o}{I_e} = \frac{-I_c}{I_e} = \frac{-h_{fe}I_b}{-(1+h_{fe})I_b} \quad \because I_c = h_{fe}\, I_b \text{ and } I_e = -(1+h_{fe})\, I_b$$

$$\therefore \quad \boxed{A_i = \frac{h_{fe}}{1+h_{fe}}} \qquad \ldots (12)$$

The above equation of CB shows that its current gain is always less than one.

Input Resistance (R_i) : It is defined as ratio of input voltage to input current

$$R_i = \frac{V_e}{I_e} = \frac{-h_{ie}I_b}{-(1+h_{fe})I_b} \qquad \because V_e = -h_{ie}\, I_b \text{ and } I_e = -(1+h_{fe})\, I_b$$

$$\boxed{R_i = \frac{h_{ie}}{1+h_{fe}}} \qquad \ldots (13)$$

Voltage Gain (A_v) : It is defined as a ratio of output to input voltages

$$A_v = \frac{V_o}{V_e} = \frac{I_o R_L}{I_e R_i} = \frac{A_i R_L}{R_i}$$

Substituting value of A_i and R_i we get,

$$\boxed{A_v = \frac{\frac{h_{fe}}{1+h_{fe}} \times R_L}{\frac{h_{ie}}{1+h_{fe}}} = \frac{h_{fe} R_L}{h_{ie}}} \quad \ldots (14)$$

Output Resistance (R_o) : It is the ratio of output voltage to output current at

$$V_s = 0$$

$$R_o = \left.\frac{V_o}{I_c}\right|_{V_s = 0}$$

When $V_s = 0$, the current through input loop $I_b = 0$, hence $I_c = 0$ and $R_o = \infty$.

The output resistance R'_o of the stage, taking the load into account is given as

$$\boxed{R'_o = R_o \parallel R_L = \infty \parallel R_L = R_L} \quad \ldots (15)$$

Comparison of amplifiers

Parameters	***Common-Emitter (CE) Amplifier***	***Common-Base (CB) Amplifier***	***Common-Collector (CC) Amplifier***
Input resistance	Moderate βr_e	Low r_e	High βR_E
Output resistance	High R_C	High R_C	Low r_e
Voltage gain	High $\frac{r_L}{r_e}$	High $\frac{r_L}{r_e}$	About 1
Current gain	High β	Low, about 1	High $(1 + \beta)$
Power gain	High	Moderate	Low
Phase shift	180°	0°	0°

Effect of coupling capacitor

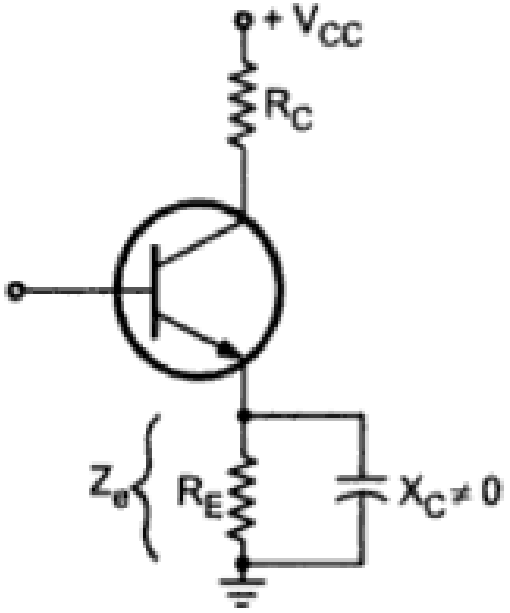
5.1.5.1 Effect of Coupling Capacitors

Recall that the reactance of a capacitor is $X_C = 1/2\pi f_C$. At medium and high frequencies, the factor f makes X_C very small, so that all coupling capacitors behave as short circuits. At low frequencies, X_C increases. This increase in X_C drops the signal voltage across the capacitor and reduces the circuit gain. As signal frequencies decrease, the capacitor reactances increase and circuit gain continues to fall, reducing the output voltage.

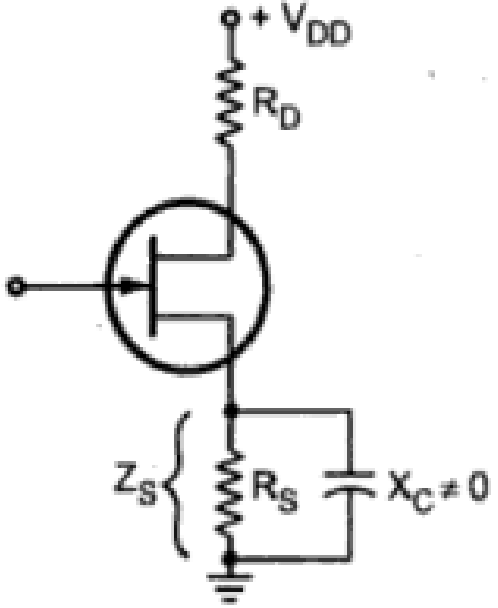
Effect of bypass capacitor in amplifier

5.1.5.2 Effect of Bypass Capacitors

At lower frequencies, the bypass capacitor C_E is not a short. So, the emitter is not at a.c. ground. X_C in parallel with R_E (R_S in case of FET) creates an impedance. The signal voltage drops across this impedance reducing the circuit gain. This is illustrated in Fig. 5.5.



(a) BJT



(b) JFET

THANK YOU