FET

BY

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INTRODUCTION

The Field Effect Transistor abbreviated as **FET** is an another semiconductor device like a BJT which can be used as an amplifier or switch. Like BJT, FET is also a three terminal device; however, the principle of operation of FET is completely different from that of BJT.

The three terminals of FET are named as Drain (D), Source (S) and Gate (G), as shown in the Fig. 3.1. Out of these three terminals gate terminal acts as a controlling terminal.

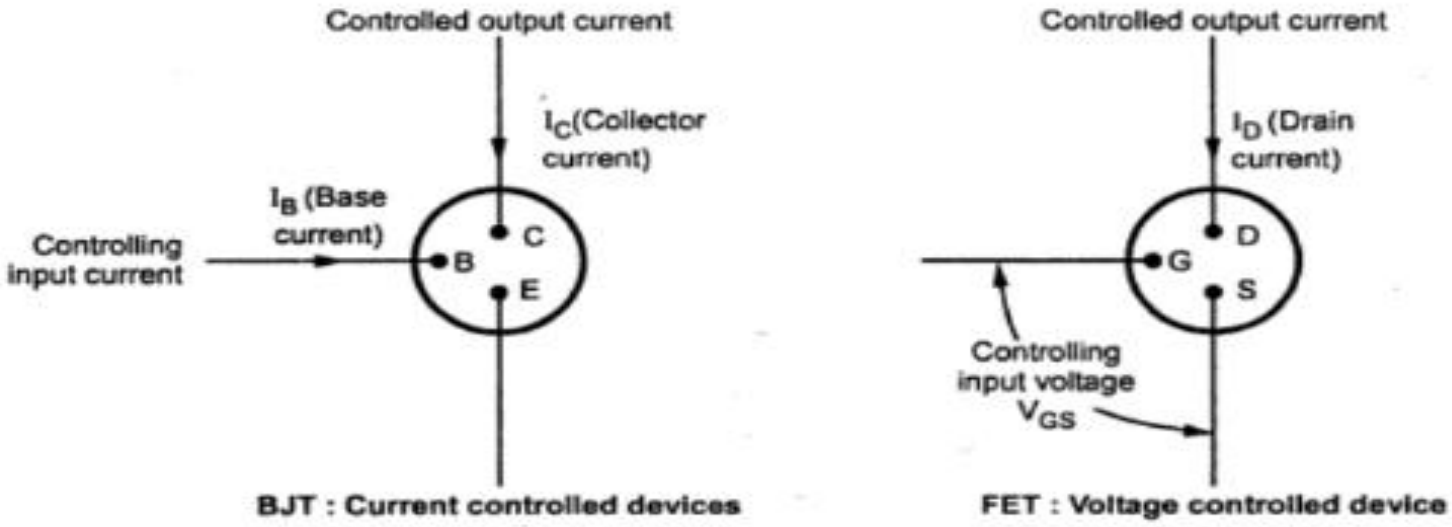


Fig. 3.1 Controlling element for BJT and FET

ADVANTAGES OF FET

- Like BJT, the parameters of FET are also temperature dependent. In FET, as temperature increases drain resistance also increases, reducing the drain current. Thus unlike BJT, thermal runaway does not occur with FET. Thus we can say that FET is **more temperature stable** as compared to the BJT.
- FET has very high input impedance. Typically, it is in the range of one to several megaohms. Because FETs have higher input impedance than BJT they are preferred in amplifiers where high input impedance is required.
- FETs require less space than that for BJTs, hence they are preferred in integrated circuits.

N-CHANNEL JFET

3.1.1.1 Structure of n-channel JFET and Symbol

The Fig. 3.3 shows structure and symbol of n-channel JFET. A small bar of extrinsic semiconductor material, n type is taken and at its two ends, two ohmic contacts are made which are the drain and source terminals of FET. Heavily doped electrodes of p type material form p-n junctions on each side of the bar. The thin region between the two p gates is called the **channel**. Since this channel is in the n type bar, the FET is known as **n-channel JFET.**

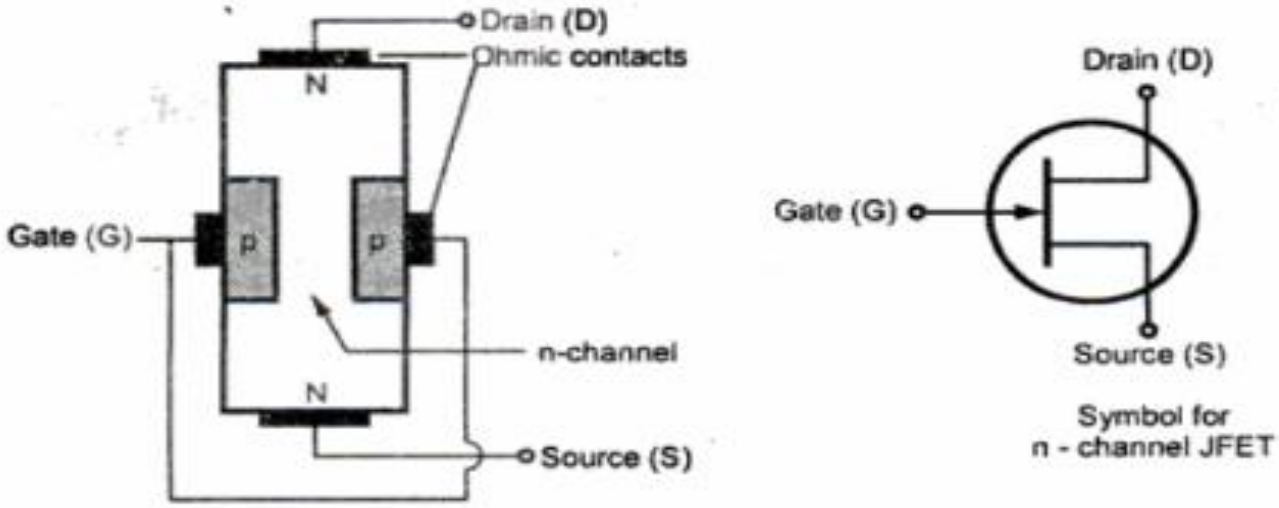


Fig. 3.3 Structure and symbol for n-channel JFET

The electrons enter the channel through the terminal called **source** and leave through the terminal called **drain**. The terminals taken out from heavily doped electrodes of p type material are called **gates**. Usually, these electrodes are connected together and only one terminal is taken out, which is called **gate**, as shown in the Fig. 3.3.

3.1.3 Principle of Operation of JFET

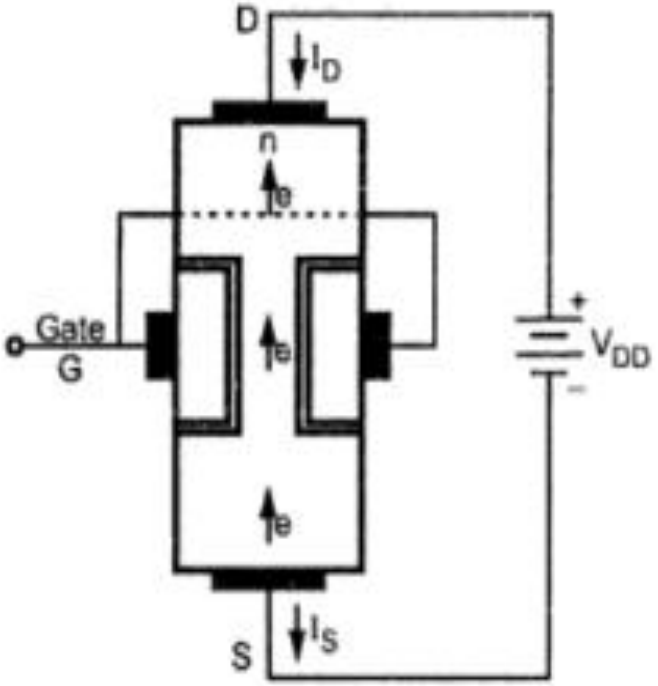
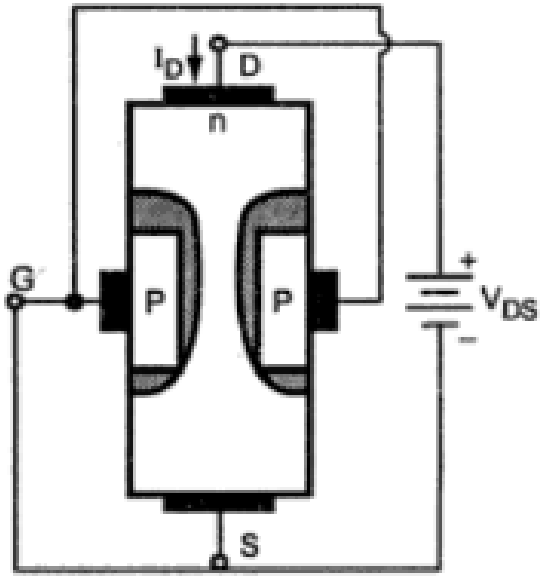


Fig. 3.6 n- channel JFET with gate open and V_{DD} is applied between drain and source

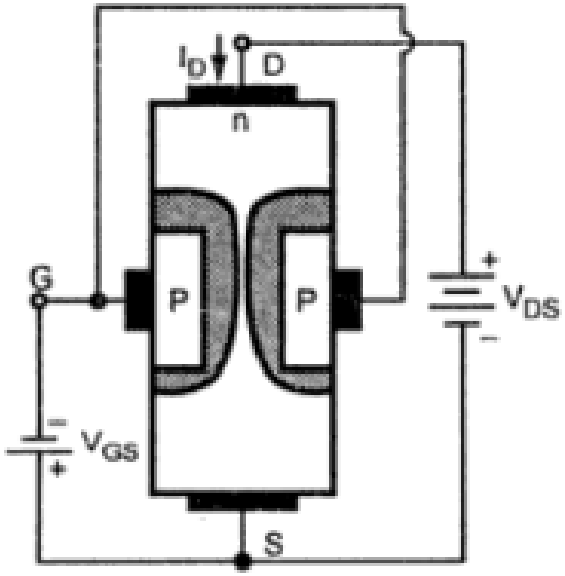
In JFET, the p-n junction between gate and source is always kept in reverse biased conditions. Since the current in a reverse biased p-n junction is extremely small, practically zero; the gate current in JFET is often neglected and assumed to be zero.

Let us consider the circuit shown in Fig. 3.6. As shown in Fig. 3.6, voltage V_{DD} is applied between drain and source. Gate terminal is kept open. The bar is of n-type material. Due to the polarities of applied voltage as shown in Fig. 3.6, the majority carriers i.e. the electrons start flowing from the source to the drain. This flow of electrons makes the drain current, I_D.

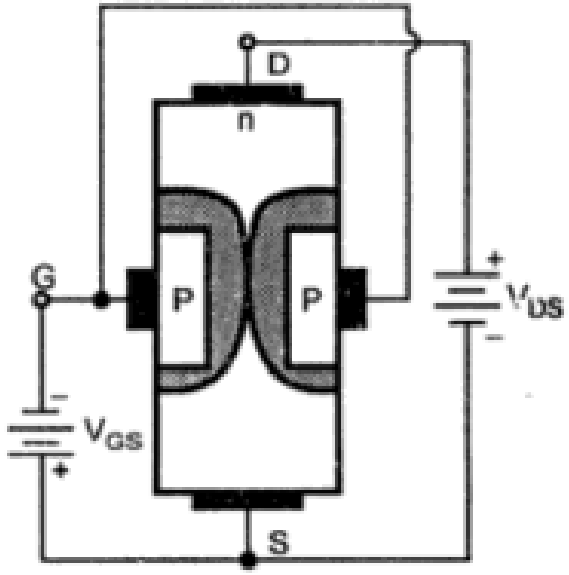
The majority carriers (electrons in n-channel JFET and holes in p-channel JFET) move from source to drain through the space between the gate regions. This space is commonly known as **channel**. The width of this channel can be controlled by varying the gate voltage. To see the effect of gate voltage on channel- width and on drain current I_D, consider the diagram shown in Fig. 3.7.



(a) No bias voltage on gates



(b) Small negative gate source bias



(c) Large negative gate source bias

Fig. 3.7 (a) shows that an n-channel JFET with the gate directly connected to the source terminal. When drain voltage V_{DS} is applied, a drain current I_D flows in the direction shown. Since the n-material is resistive, the drain current causes a voltage drop along the channel. This voltage drop reverse biases the pn junctions and causes the depletion regions to penetrate into the channel. Since gate is heavily doped and the channel is lightly doped, the width of the depletion region will mainly be spread in the channel shown in the Fig. 3.7 (a). This penetration depends on the reverse bias voltage. Looking at Fig. 3.7 (a) we can observe that depletion region width is more at the drain side as compared to source side because near the junction, voltage at drain side is more than the voltage at the source side. This shows that reverse bias is not uniform near the junction; it gradually increases from source side to drain side.

JFET AS VCCS

JFET as Voltage Controlled Current Source

As we know, depletion region does not contain charge carriers, the space between two depletion regions is available for the conducting portion of the channel. If we externally apply reverse bias voltage to the gate, the reverse bias will further increase and hence increase the penetration of the depletion region, which reduces the width of the conducting portion of the channel. As width of the conducting portion of the channel reduces, the number of electrons flowing from source to drain reduces and hence the current flowing from drain to source reduces. If we go on increasing the reverse bias voltage to the gate as shown in Fig. 3.7 (b) and 3.7 (c), depletion regions will increase more and more and stage will come when the width of the depletion regions will be equal to the original width of the channel, leaving zero width for conducting portion of the channel, as shown in the Fig. 3.7 (c). This will prevent any current flow from drain to source and this will cut off the drain current. The gate to source voltage that produces cutoff is known as **cutoff voltage** and it is denoted by $V_{GS\,(off)}$.

When the gate is shorted to source, there is minimum reverse bias between gate and source p-n junction, making depletion region width minimum and conducting channel width maximum. In this case maximum drain current flows which is designated by I_{DSS} and this is the maximum possible drain current in JFET. From above discussion it is cleared that the gate to source voltage controls the current flowing through channel and hence FET is also called **voltage controlled current source.**

Key Point : *The JFET is always operated with gate-source p-n junction reverse-biased.*

JFET CHARACTERISTICS

To understand electrical behaviour of a JFET, it is necessary to study the interrelation of the current and voltages in JFET. These relationships can be plotted graphically which are commonly known as the characteristics of JFET. The important characteristics of JFET are drain characteristics and transfer characteristics. The following section explains these characteristics in detail.

3.2.1 Drain V-I Characteristics for n-channel JFET

Fig. 3.8 shows the drain characteristics of a n-channel JFET. The curves represent relationship between the drain current I_D and drain to source voltage V_{DS} for different values of V_{GS}. Fig. 3.9 shows the experimental setup required to plot this characteristics.

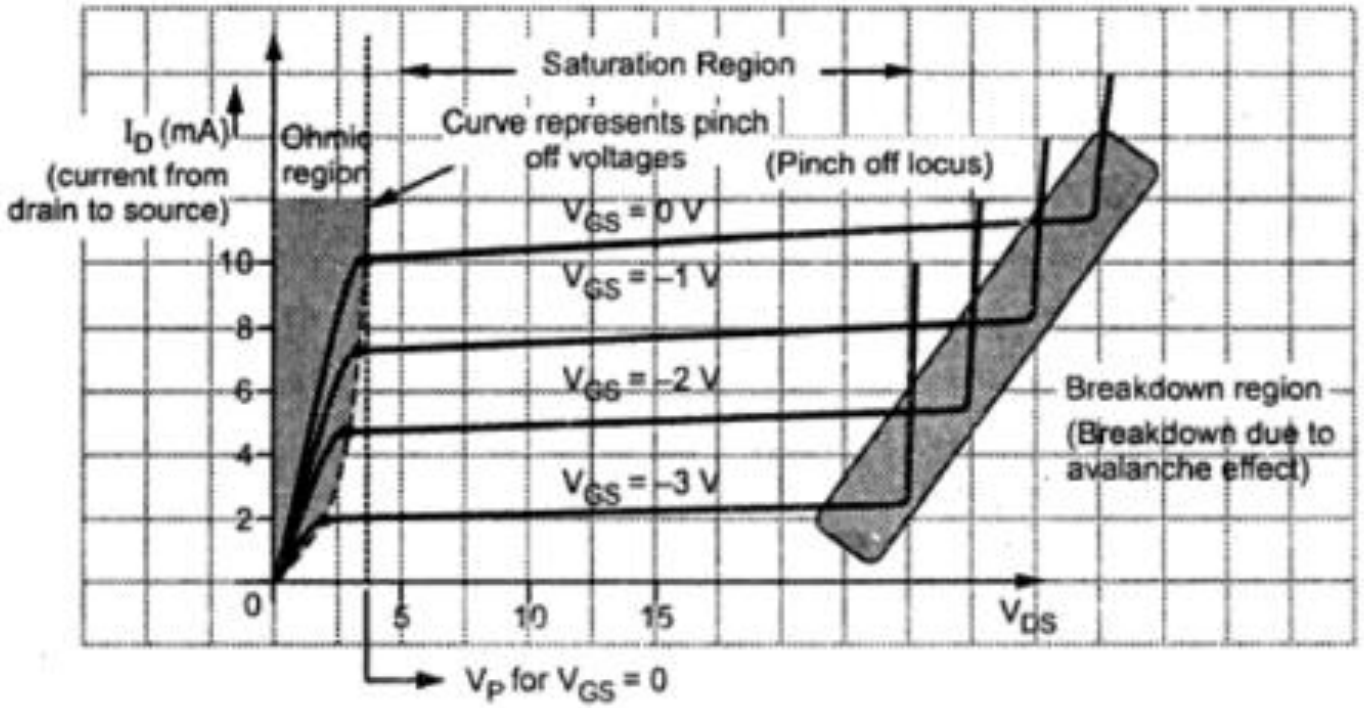


Fig. 3.8 Drain V-I characteristics of n-channel JFET

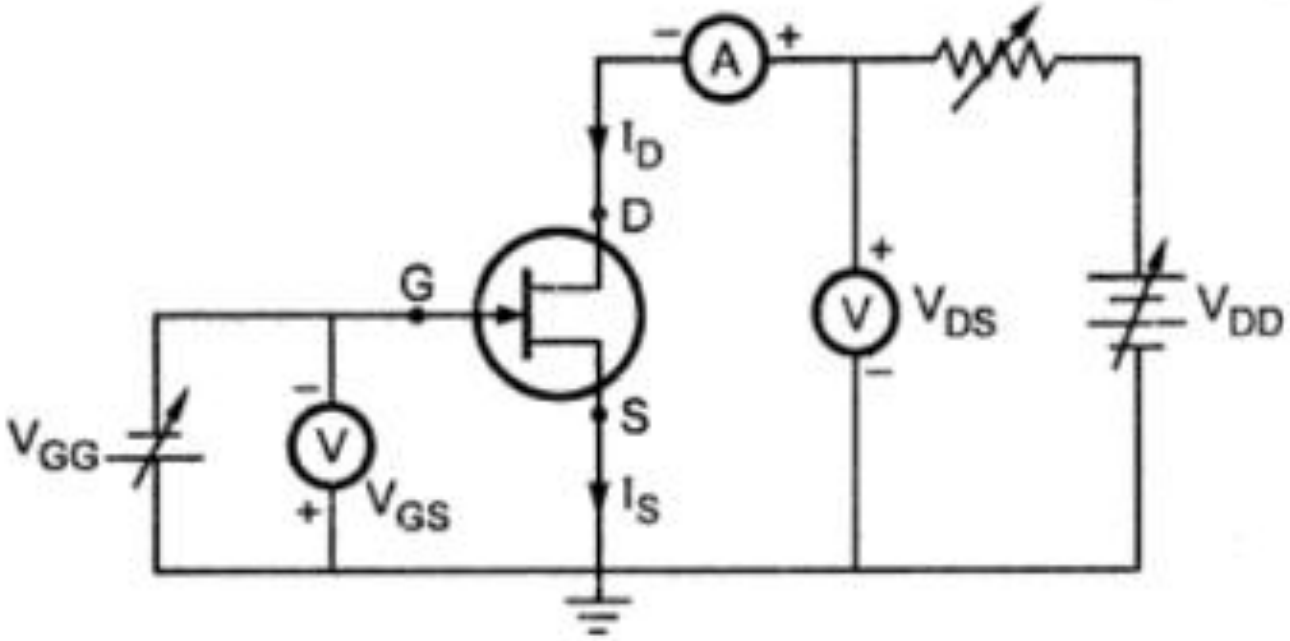


Fig. 3.9 Experimental setup to plot JFET characteristics

1. V_{GS} and V_{DS} both = 0 :

When $V_{GS} = 0$ the channel is entirely open. But $V_{DS} = 0$, so there is no attractive force for the majority carriers (electrons in n-channel JFET) and hence drain current does not flow.

2. Self pinch off at no bias ($V_{GS} = 0$) :

At $V_{GS} = 0$, in response to a small applied voltage V_{DS}, the n-type bar acts as a simple semiconductor resistor and the current I_D increases linearly with V_{DS}. As V_{DS} increases, the voltage drop along the channel also increases. This increase in voltage drop increases the reverse bias on gate-source junction and causes the depletion regions to penetrate into the channel, reducing channel width. The effect of reduction in channel width provides more opposition to increase in drain current I_D. Thus, rate of increase in I_D with respect to V_{DS} is now reduced. This is shown by the curved shape in the characteristics.

At some value of V_{DS}, drain current I_D cannot be increased further, due to reduction in channel width. Any further increase in V_{DS} does not increase the drain current I_D. I_D approaches the constant saturation value. The voltage V_{DS} at which the current I_D reaches to its constant saturation level is called **'Pinch-Off Voltage'**, V_p.

The pinch off voltage V_P is given by

$$|V_P| = \frac{qN_D}{2\epsilon} a^2$$

where

ϵ : Dielectric constant of channel material. For silicon $\epsilon = 12\,\epsilon_o (\epsilon_o = 8.849 \times 10^{-12}$ F/m)

a : Half the region of n-type material without considering channel width in meters

N_D : Concentration of donar atoms electron/m^3

q : Electronic charge = 1.6×10^{-19} C

3. V_{GS} with negative bias :

When an external bias, of say –1 V, is applied between the gate and the source, the gate channel junctions are further reverse biased, reducing the effective width of the channel available for the conduction. Because of this, drain current will reduce and pinch off voltage is reached at a lower drain current than when $V_{GS} = 0$, as shown in Fig. 3.8.

By applying several values of negative external bias voltage (V_{GS}), a family of curves are obtained as shown in Fig. 3.8. From Fig. 3.8 it can be observed that for more negative values of V_{GS}, the pinch-off voltage is reached at lesser values of I_D.

The V_{GS} is given by,

$$V_{GS} = \left(1 - \frac{b}{a}\right)^2 V_P \quad \text{where b : half channel width}$$

4. Breakdown region :

We can observe from the Fig. 3.8 that if we increase value of V_{DS} beyond pinch off voltage, V_p, the drain current I_D remains constant, upto certain value of V_{DS}. If we further exceed V_{DS}, the voltage will be reached at which the gate-channel junction breaks down, due to avalanche effect. At this point the drain current increases very rapidly and the device may be destroyed.

It can be observed that the values of V_{DS} for break down are reduced as the negative gate bias is increased. This is because the total **reverse breakdown voltage** is the addition of the reverse voltage due to self pinch-off and the externally applied voltage V_{GS}.

5. Ohmic and saturation regions :

It is seen that the drain characteristics of JFET is divided into two regions : ohmic region and saturation region. In the ohmic region, the drain current I_D varies with V_{DS} and the JFET is said to behave as **voltage variable resistance**. In the saturation region, the drain current I_D remains fairly constant and does not vary with V_{DS}. Saturation in a FET refers to the limiting value to drift velocity. Thus the number of carriers that can be transported through the channel per unit time is limited or saturated and I_D remains constant. This is a very different meaning of saturation than that encountered for BJT. To use FET as an amplifier, it is operated in this saturation region.

6. Cut-off :

As we know, for an n-channel JFET, the more negative V_{GS} causes drain current to reduce and pinch off voltage to reach at a lower drain current. When V_{GS} is made sufficiently negative, I_D is reduced to 0, as shown in the Fig. 3.10. This is caused by the widening of the depletion region to a point where it completely closes the channel. The value of V_{GS} at the cutoff point is designated as $V_{GS(OFF)}$.

3.2.3 Transfer Characteristics for n-channel JFET

Fig. 3.12 shows the transfer characteristics of n-channel JFET. The curves represents relationship between the drain current I_D and gate to source voltage V_{GS}.

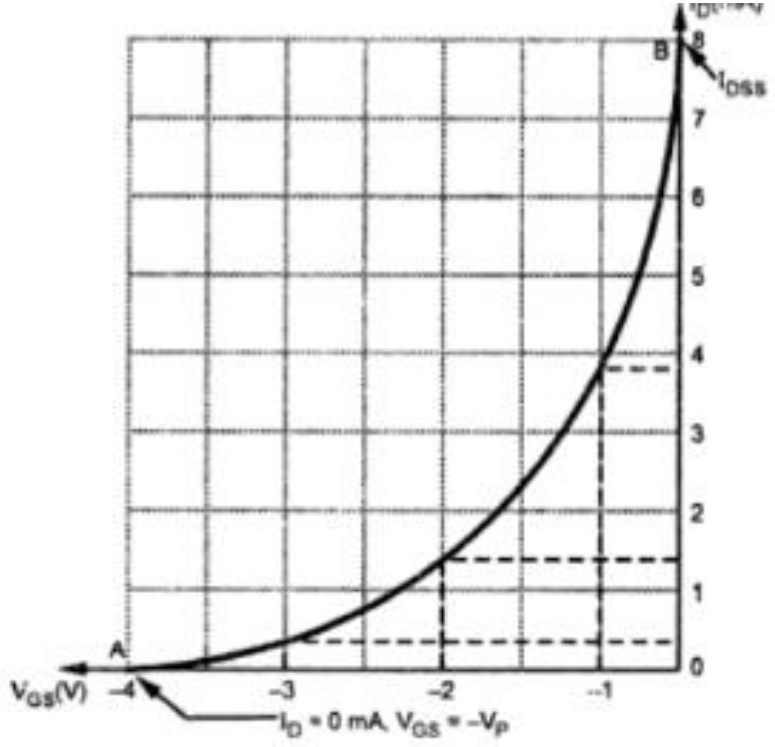


Fig. 3.12 Transfer characteristics of n-channel JFET

From this characteristics we observe following points :

1. The relationship between the drain current I_D and gate to source voltage V_{GS} is non-linear. This relationship is defined by **Shockley's** equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 \quad \ldots (1)$$

The squared term of the equation will result in a non-linear relationship between I_D and V_{GS}, producing a curve that grows exponentially with decreasing magnitudes of V_{GS}. From equation we can also write,

$$V_{GS} = V_p\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right) \quad \ldots (2)$$

In the equation values of I_{DSS} and V_p are constants, value of V_{GS} controls I_D .

2. A point A at the bottom end of the curve on the V_{GS}-axis represents $V_{GS\,(off)}$ and point B at the top end of the curve on the I_D axis represents I_{DSS} (maximum drain current at $V_{GS} = 0$). Thus, this curve shows the operating limits of a JFET.

These are : $I_D = 0$ when $V_{GS} = V_{GS\,(off)}$

$I_D = I_{DSS}$ when $V_{GS} = 0$

Example 3.1 : *Data sheet for a JFET indicates that $I_{DSS} = 10\ mA$ and $V_{GS(off)} = -4\ V$. Determine the drain current for $V_{GS} = 0\ V, -1\ V$ and $-4\ V$.*

Solution : For $V_{GS} = 0\ V$, $I_D = I_{DSS} = 10\ mA$

For $V_{GS} = -1$, using equation (1) we have

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = 10\ mA\left(1 - \frac{-1}{-4}\right)^2$$

$$= 10 \times 10^{-3}\,[1 - 0.25]^2 = 10 \times 10^{-3} \times 0.5625 = \mathbf{5.625\ mA}$$

For $V_{GS} = -4\ V$

$$I_D = 10\ mA\left(1 - \frac{-4\ V}{-4\ V}\right)^2 = 10 \times 10^{-3}\,(1-1)^2$$

$$= 10 \times 10^{-3}\,(0)^2 = \mathbf{0\ mA}$$

3.3 JFET Parameters

The important parameters of JFET are as follows :

- Transconductance (g_m)
- Input resistance and capacitance
- Drain to source resistance (r_d)
- Amplification factor (μ)

3.3.1 Transconductance

The transconductance, g_m, is the change in the drain current for given change in gate to source voltage with the drain to source voltage constant as shown in Fig. 3.17.

Looking at Fig. 3.17, we can say that it is the slope of the transfer characteristic. Since the slope varies, g_m also varies. g_m has a greater value near the top of the curve than it does near the bottom. The transconductance g_m is defined as

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS\ constant}} \quad \ldots (1)$$

The transconductance g_m is also called **mutual conductance.** The practical unit for g_m is mS (millisiemen) or mA/V. For given g_m, we can calculate an approximate value for g_m at any point on the transfer characteristic curve using the following equation

$$\boxed{g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]} \quad \ldots (2)$$

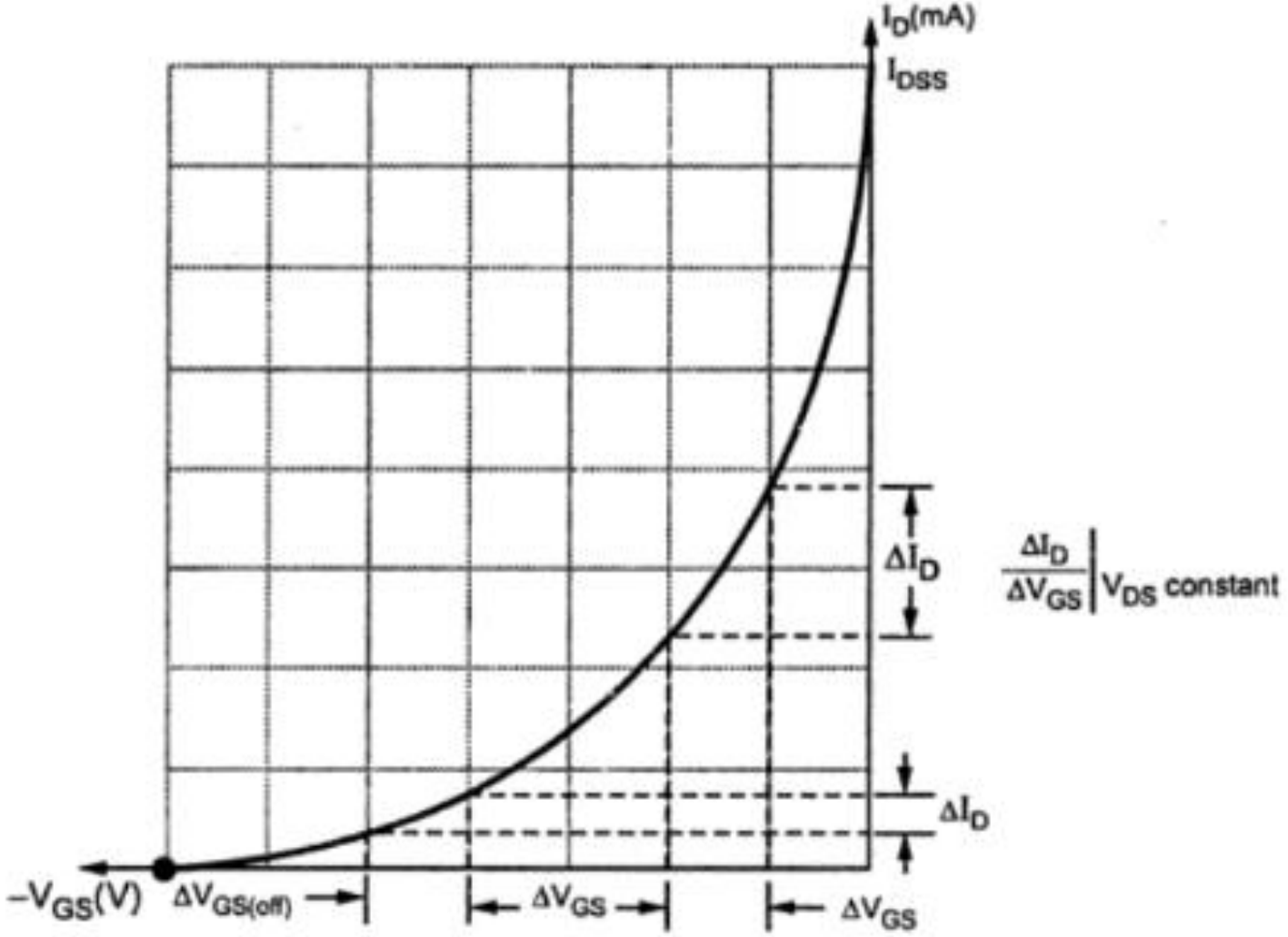


Fig. 3.17 Transconductance g_m varies depending on the bias point (V_{GS})

Where g_{mo} is the value of g_m for $V_{GS} = 0$ and is given by,

$$g_{mo} = \frac{-2 I_{DSS}}{V_p} \qquad \ldots(3)$$

This can be proved as given below. We know that,

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2$$

Differentiating this equation with respect to V_{GS} we get,

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{-2 I_{DSS}}{V_p}\left[1 - \frac{V_{GS}}{V_p}\right]$$

$$= g_{mo}\left[1 - \frac{V_{GS}}{V_p}\right] \qquad \text{where} \quad g_{mo} = \frac{-2 I_{DSS}}{V_p}$$

Input Resistance and Capacitance

We know that a JFET operates with its gate source junction reverse-biased. Therefore, the input resistance at the gate is very high. This high input resistance is one advatnage of the JFET over the bipolar transistor. (Recall that a BJT operates with a forward biased base-emitter junction.) JFET data sheets often specify the input resistance by giving a value of the gate reverse current, I_{GSS}, at a cetain gate to surce voltage, V_{GS}. The input resistance can then be determined using the following equation, where the vertical lines indicate an absolute value.

$$R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right|$$

Drain to Source Resistance

The drain resistance r_d is the a.c. resistance between drain and source terminals when the JFET is operating in the saturation region. It is the reciprocal of the slope of the drain characteristic in the saturation region. It is given by

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS} \text{ constant}}$$

Amplification Factor

The amplification factor, denoted by μ is defined as,

$$\text{Amplification factor } \mu = \left.\frac{\Delta V_{DS}}{\Delta V_{GS}}\right|_{I_D \text{ constant}}$$

$$\therefore \quad \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

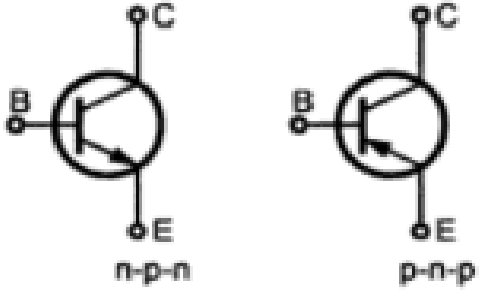
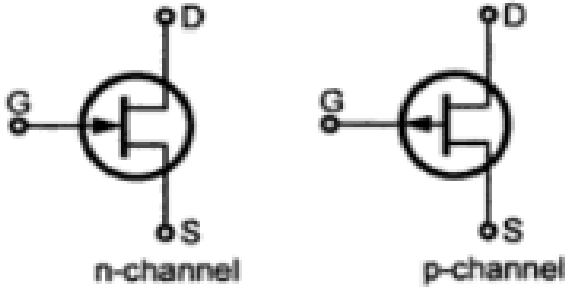
$$\therefore \qquad \boxed{\mu = r_d \times g_m} \qquad \ldots(5)$$

Key Point : *Since the parameter μ is the ratio of two similar quantities viz. ratio of two voltages; μ is unitless.*

COMPARISION OF BJT & FET

BJT	FET
CURRENT CONTROLLED DEVICE	VOLTAGE CONTROLLED DEVICE
BIPOLAR DEVICE	UNIPOLAR DEVICE
THERMAL RUNAWAY TAKES PLACE	NO THERMAL RUNAWAY
LOW INPUT IMPEDANCE	HIGH INPUT IMPEDANCE
NOISE GENERATED IS HIGH	NOISE GENERATED IS LOW
BIG IN SIZE	SMALL IN SIZE
TRANSCONDUCTANCE IS HIGH	LOWER THAN BJT
APPLICATION: AS SWITH –SATURATION & CUTOFF REGION AS AMPLIFIER- ACTIVE REGION	APPLICATION: AS SWITH –OHMIC & CUTOFF REGION AS AMPLIFIER- ACTIVE REGION

COMPARISON

Sr. No.	Parameter	BJT	FET
1.	**Control element**	Current controlled device. Input current I_B controls output current I_C.	Voltage controlled device. Input voltage V_{GS} controls drain current I_D.
2.	**Device type**	Current flows due to both, majority and minority carriers and hence **bipolar device.**	Current flows only due to majority carriers and hence **unipolar device.**
3.	**Types**	n-p-n and p-n-p	n-channel and p-channel.
4.	**Symbols**		
5.	**Configurations**	CE, CB, CC	CS, CG, CD

6.	**Input resistance**	Less compare to JFET.	High compare to BJT.
7.	**Size**	Bigger than JFET.	Smaller in construction than BJT, thus making them useful in integrated - circuits (IC).
8.	**Sensitivity**	Higher sensitivity to changes in the applied signals.	Less sensitivity to changes in the applied voltage.
9.	**Thermal stability**	Less	More

APPLICATION OF FET

3.6 Use of JFET as a VVR or VDR

Let us consider the drain characteristics of FET as shown in the Fig. 3.35. In this characteristics we can see that in the region before pinch off voltage, drain characteristics is linear, i.e. FET operation is linear. In this region the FET is useful as a voltage-controlled resistor, i.e., the drain to source resistance is controlled by the bias voltage V_{GS}. The operation of FET in this region is useful in most linear applications of FET. In such an application the FET is also referred to as a **voltage-variable resistor (VVR)** or **voltage-dependent resistor (VDR)**.

Application

The voltage variable resistor property of FET can be used to vary the voltage gain of a multistage amplifier A as the signal level is increased. This action is called automatic gain control (AGC). This is illustrated in Fig. 3.36. Here, maximum value of signal is taken, rectified and filtered to produce a d.c. voltage proportional to the output signal level. This voltage is applied to the gate of JFET, thus causing the a.c. resistance between the drain and source to change. As this resistance is connected across R_E, effective R_E also changes according to change in the drain to source resistance. When output signal level increases, the drain to source resistance also increases, increasing effective R_E. Increase in R_E causes the gain of transistor Q_1 to decrease reducing the output signal. Exactly reverse process takes place when output signal level decreases. Therefore, the output signal level is maintained constant. It is important to note that the d.c. bias conditions of Q_1 are not affected by JFET since FET is isolated from Q_1 by means of capacitor C_2.

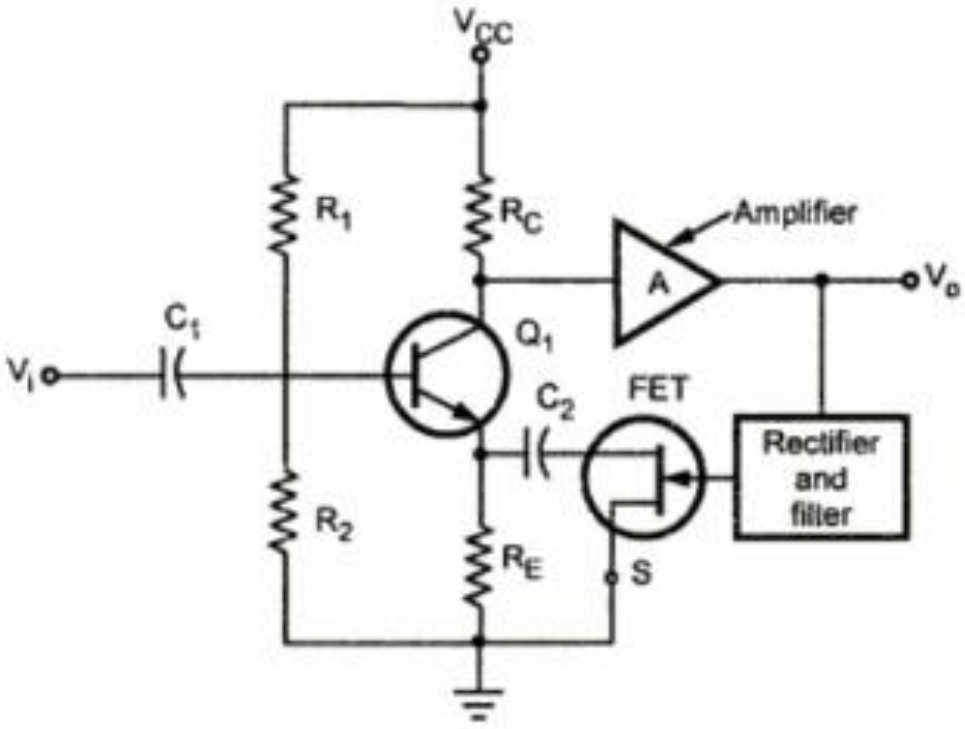


Fig. 3.36 AGC amplifier using FET as a voltage variable resistor

MOSFET

The MOSFET differs from the JFET in that it has no p-n junction structure ; instead, the gate of the MOSFET is insulated from the channel by a silicon dioxide (SiO_2) layer. Due to this the input resistance of MOSFET is greater than JFET. Because of the insulated gate, MOSFETs are also called **IGFETs**.

DEPLETION MOSFET

3.7.1.1 Construction of n-channel MOSFET

The Fig. 3.37 shows the basic construction of n-channel depletion type MOSFET. Two highly doped n-regions are diffused into a lightly doped p-type substrate. These two highly doped n-regions represent source and drain. In some cases substrate is internally connected to the source terminal.

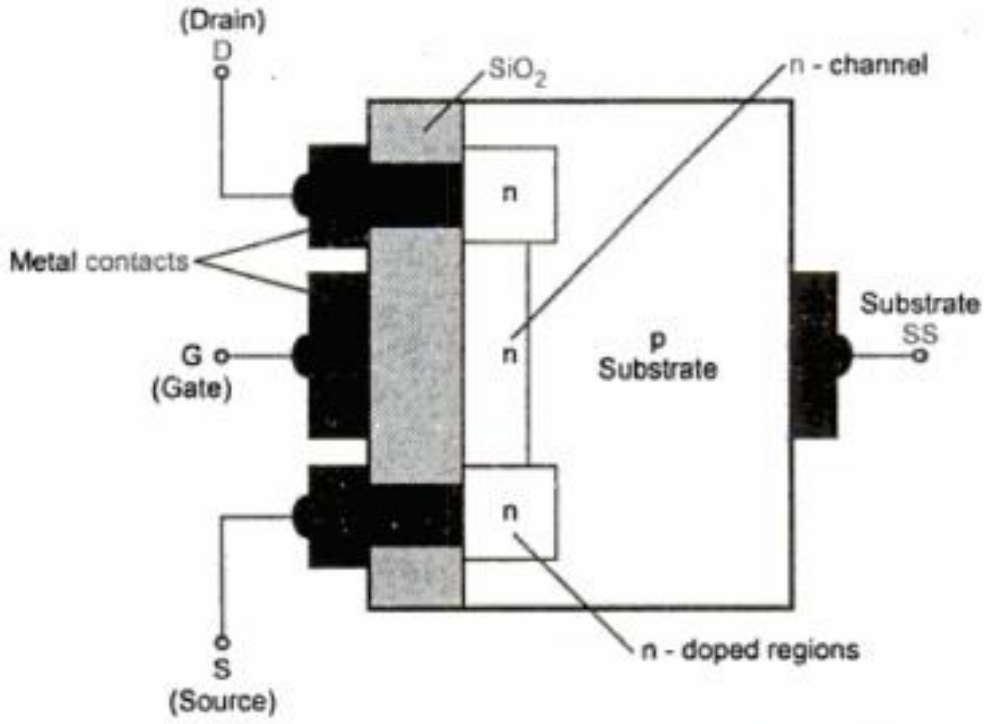


Fig. 3.37 n-channel depletion-type MOSFET

The source and drain terminals are connected through metallic contacts to n-doped regions linked by an n-channel as shown in the Fig. 3.37. The gate is also connected to a metal contact surface but remains insulated from the n-channel by a very thin layer of dielectric material, silicon dioxide (SiO_2). Thus, there is no direct electrical connection between the gate terminal and the channel of a MOSFET, increasing the input impedance of the device.

3.7.1.2 Operation, Characteristics and Parameters of n-channel MOSFET

On the application of drain to source voltage, V_{DS} and keeping gate to source voltage to zero by directly connecting gate terminal to the source terminal, free electrons from the n-channel are attracted towards positive potential of drain terminal. This establishes current through the channel to be denoted as I_{DSS} at $V_{GS} = 0$ V, as shown in the Fig. 3.38.

If we apply negative gate voltage, the negative charges on the gate repel conduction electrons from the channel, and attract holes from the p-type substrate. This initiates recombination of repelled electrons and attracted holes as shown in the Fig. 3.39.

The level of recombination between electrons and holes depends on the magnitude of the negative voltage applied at the gate. This recombination reduces the number of free electrons in the n-channel for the conduction, reducing the drain current.

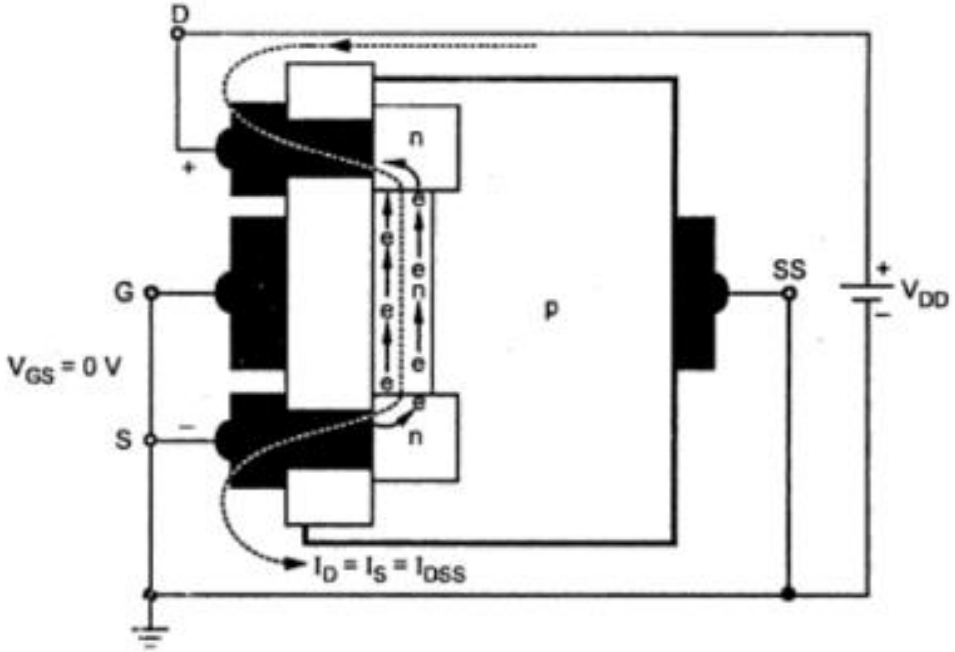


Fig. 3.38 N-channel depletion-type MOSFET with V_{GS}= 0V and an applied voltage V_{DD}

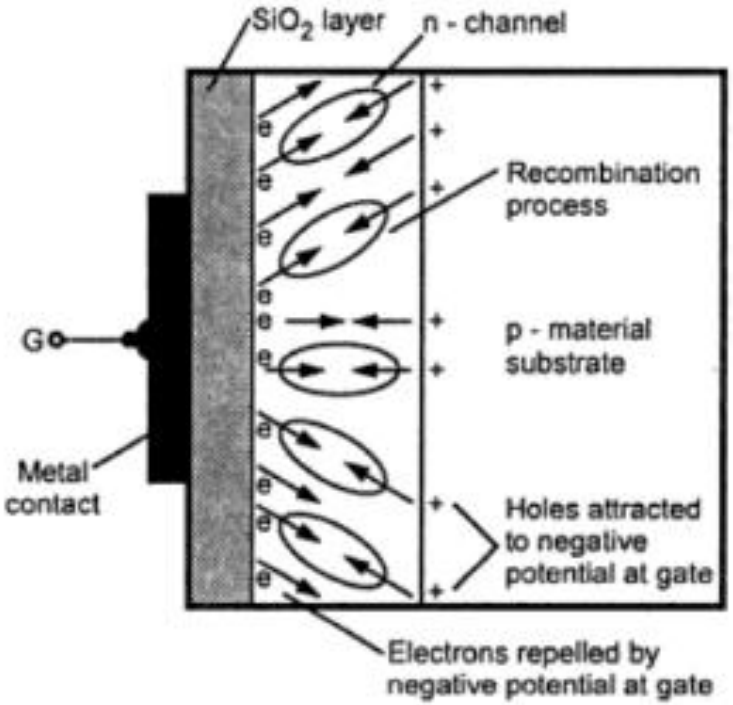


Fig. 3.39 Reduction in free electrons in the n-channel due to negative potential at the gate terminal

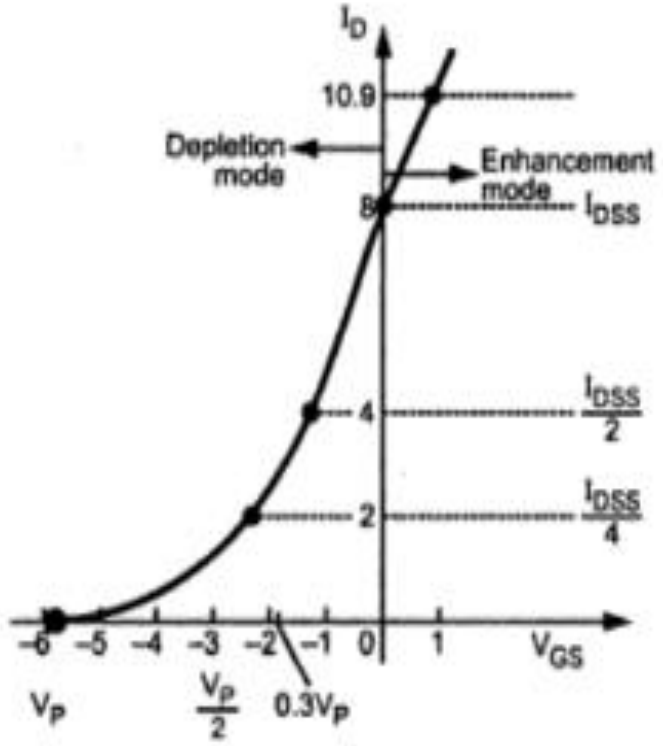


Fig. 3.40 Transfer characteristics for an n-channel depletion type MOSFET

In other words we can say that, due to recombinations, n-channel is depleted of some of its electrons, thus decreasing the channel conductivity. The greater the negative voltage applied at the gate, the greater the depletion of n-channel electrons. The level of drain current will reduce with increasing negative bias for V_{GS} as shown in the transfer characteristics of depletion type MOSFET (Fig. 3.40).

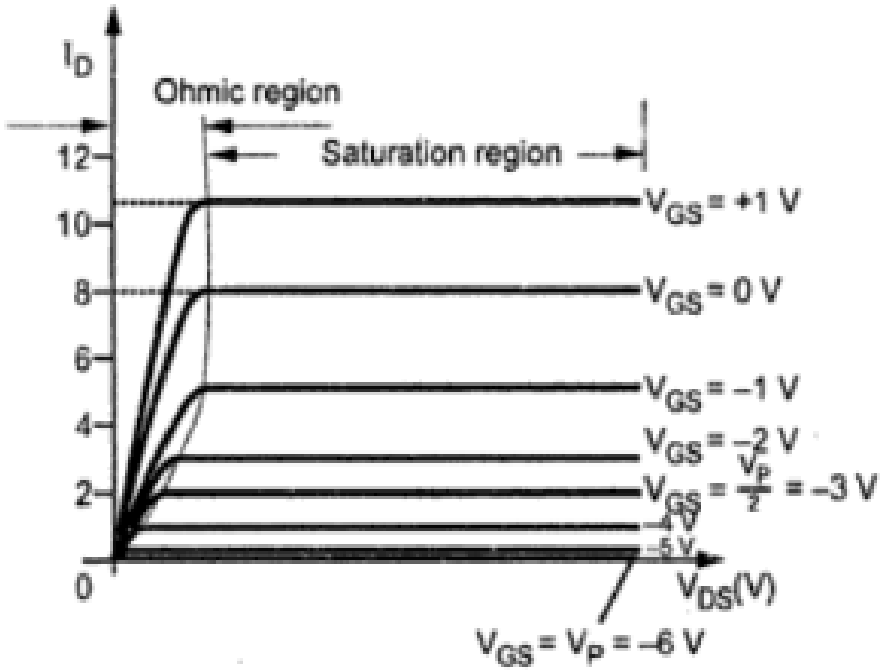
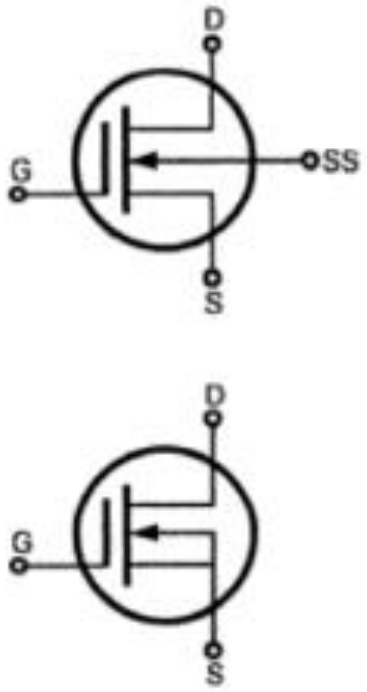


Fig. 3.41 Drain characteristics for an n-channel depletion type MOSFET

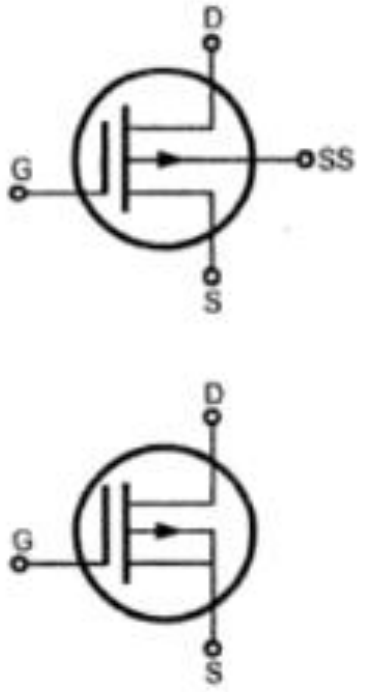
For positive values of V_{GS} the positive gate will draw additional electrons from the p-type substrate due to reverse leakage current and establish new carriers through the collisions between accelerating particles. Because of this, as gate to source voltage increases in positive direction, the drain current also increases as shown in the Fig. 3.40.

The application of a positive gate to source voltage has "enhanced" the level of free carriers in the channel compared to that encountered with V_{GS} = 0 V. For this reason the region of positive gate voltages on the drain or transfer characteristics is referred to as enhancement region and the region between cutoff and the saturation levels of I_{DSS} referred to as depletion region. Fig. 3.41 shows drain characteristics for an n-channel depletion type MOSFET. It is similar to that of JFET. The only difference is that it has positive part of V_{GS} .

SYMBOLS OF D-MOSFET



(a) Symbols for n-channel depletion type MOSFETs



(b) Symbols for p-channel depletion type MOSFETs

3.7.2 Enhancement MOSFET (E-MOSFET)

This type of MOSFET operates only in the enhancement mode and has no depletion mode. It differs in construction from the depletion MOSFET in that it has no physical channel.

3.7.2.1 Construction of n-channel E-MOSFET

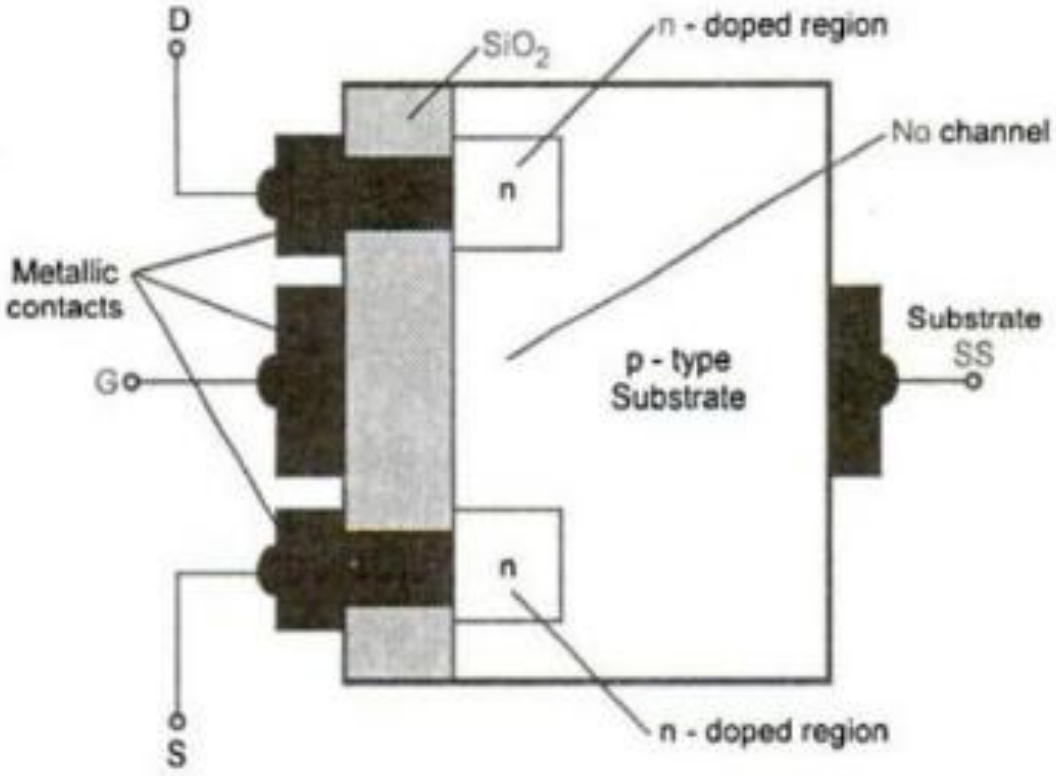


Fig. 3.44 n-channel enhancement type MOSFET

The Fig. 3.44 shows the basic construction of n-channel enhancement type MOSFET.

Like, depletion type MOSFET, two highly doped n-regions are diffused into a lightly doped p-type substrate. The source and drain are taken out through metallic contacts to n-doped regions as shown in the Fig. 3.44. But the channel between two n-regions is absent in the enhancement type MOSFET. The SiO_2 layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the p-type material.

3.7.2.2 Operation, Characteristics and Parameters of n-channel E-MOSFET

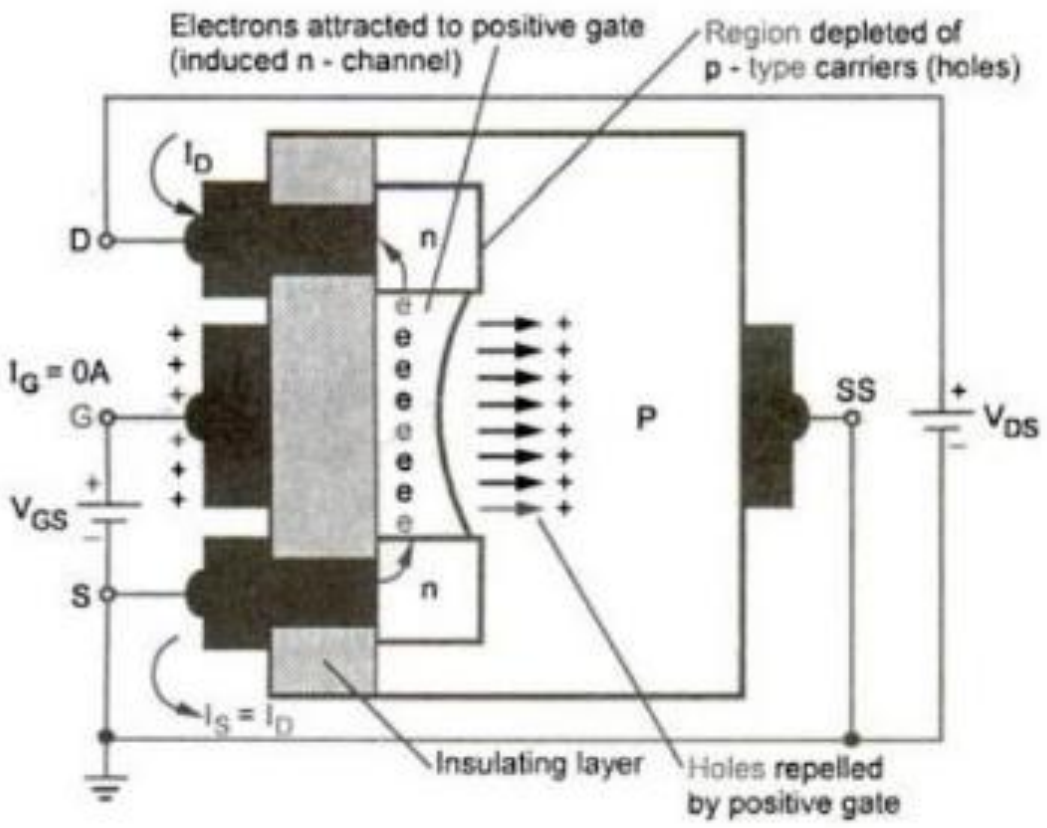


Fig. 3.45 Channel formation in the n-channel enhancement type MOSFET

On application of drain to source voltage V_{DS} and keeping gate to source voltage zero by directly connecting gate terminal to the source terminal, practically zero current flows-quite different from the depletion type MOSFET and JFET. If we increase magnitude of V_{GS} in the positive direction, the concentration of electrons near the SiO_2 surface increases. At a particular value of V_{GS} there is a measurable current flow between drain and source. This value of V_{GS} is called threshold voltage denoted by V_T. Thus we can say that in an

enhancement type n-channel MOSFET, a positive gate voltage above a threshold value induces a channel and hence the drain current by creating a thin layer of negative charges in the substrate region adjacent to the SiO_2 layer, as shown in the Fig. 3.45. The conductivity of the channel is enhanced by increasing the gate to source voltage and thus pulling more electrons into the channel. For any voltage below the threshold value, there is no channel.

Since the channel does not exist with $V_{GS} = 0$ V and "enhanced" by the application of a positive gate to source voltage, this type of MOSFET is called an enhancement type MOSFET.

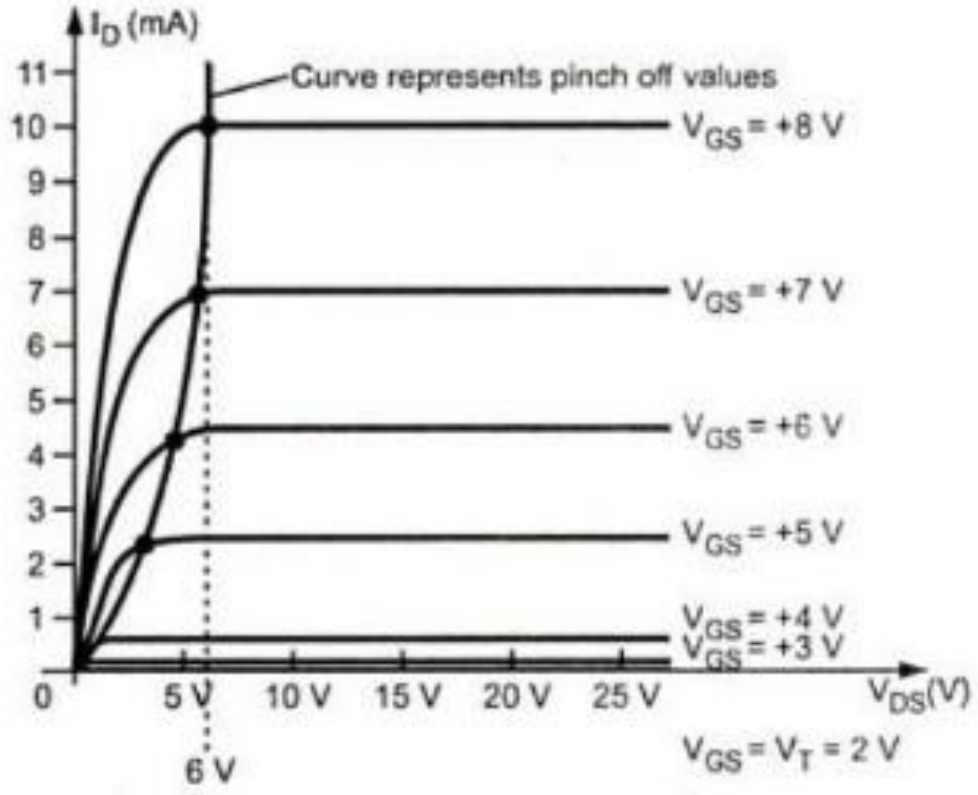


Fig. 3.46 Drain characteristics of an n-channel enhancement type MOSFET

Fig. 3.46 shows the drain characteristics of an n-channel enhancement type MOSFET. Looking at Fig. 3.46 we can say that as V_{GS} increases beyond the threshold level, the density of free carriers (electrons) in the induced channel increases, increasing the drain current. However, at some point of V_{DS}, for constant V_{GS}, the drain current reaches a saturation level. The levelling off of I_D is due to a pinch-off process, is as described earlier for the JFET. Fig. 3.47 shows pinch off process for n-channel enhancement type MOSFET.

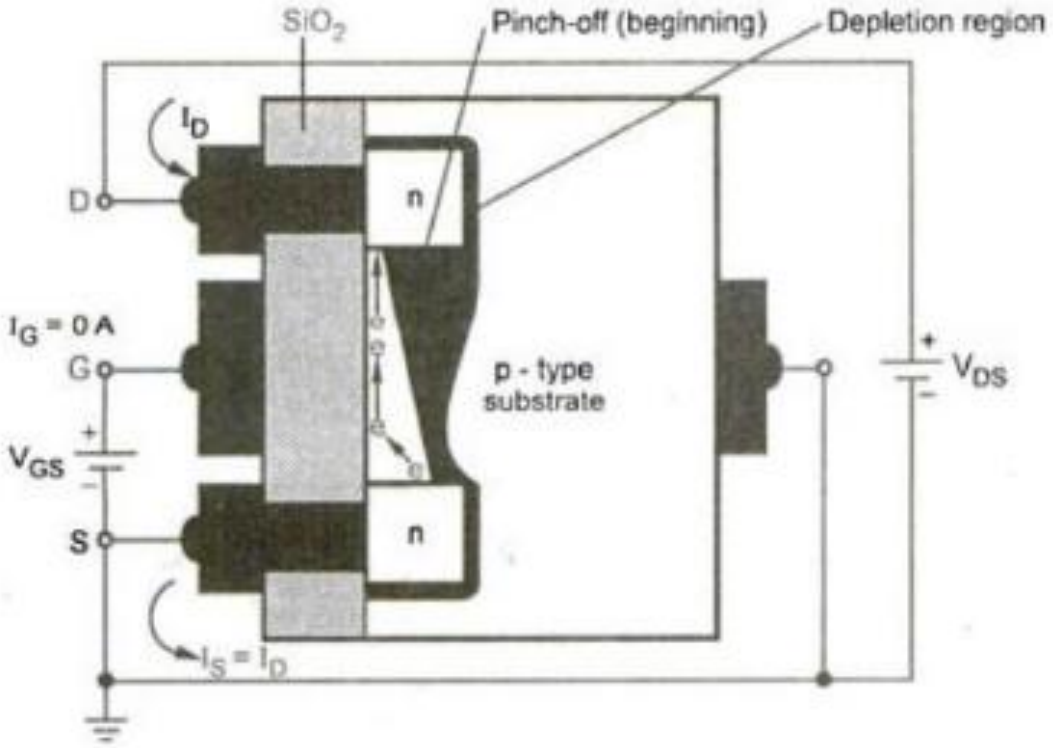


Fig. 3.47 Change in channel and depletion region with increasing level of V_{DS} for a fixed value of V_{GS}

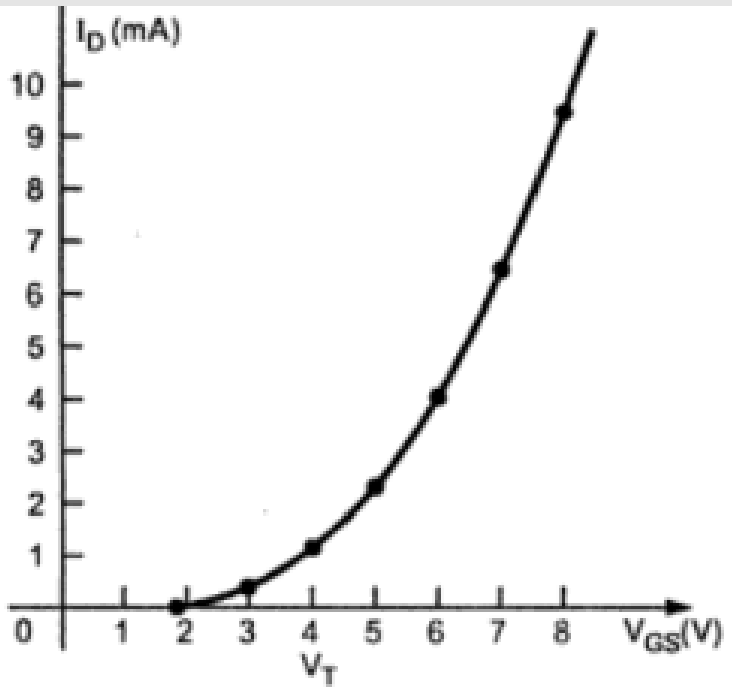


Fig. 3.48 Transfer characteristic for n-channel enhancement type MOSFET

characteristic for n-channel enhancement type MOSFET. This characteristic is quite different from characteristic that we obtained for JFET and depletion type MOSFET. For an n-channel enhancement type MOSFET it is now totally in the positive V_{GS} region and as we know I_D does not flow until $V_{GS} = V_T$.

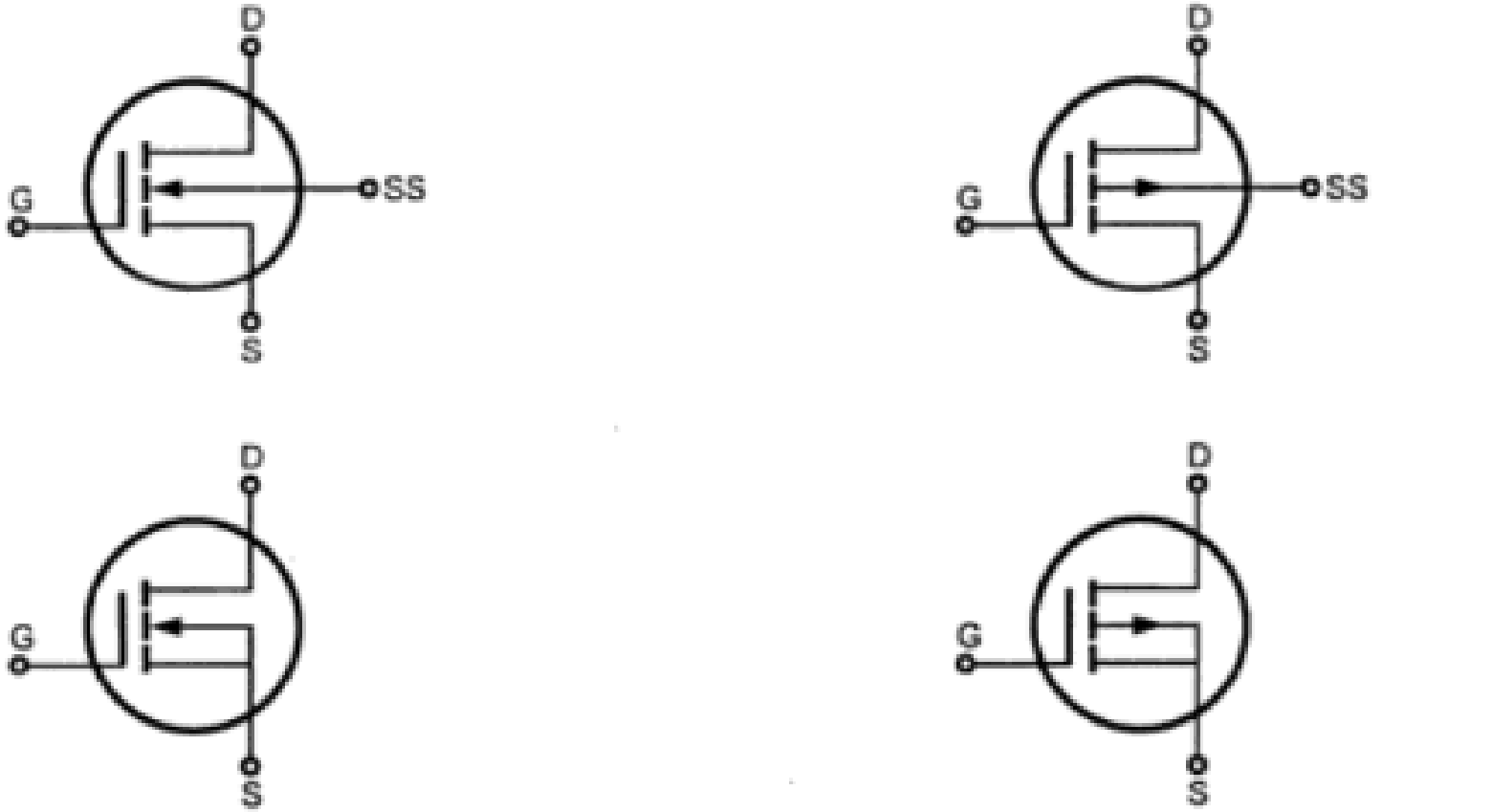
For $V_{GS} > V_T$ the relationship between drain current and V_{GS} is nonlinear and it is given as

$$I_D = K(V_{GS} - V_T)^2 \qquad \ldots (1)$$

The K term is a constant that is a function of the construction of the device. The value of K can be determined from equation,

$$K = \frac{I_{D(ON)}}{(V_{GS(ON)} - V_T)^2} \qquad \ldots (2)$$

E-MOSFET SYMBOLS



(a) Symbols for n-channel type MOSFETs enhancement

(b) Symbols for p-channel type MOSFETs enhancement

Fig. 3.52 Symbols

COMPARISION OF JFET & MOSFET

S.No	JFET	MOSFET
1	Operated in depletion mode	Operated in depletion mode and enhancement mode
2	High input impedance(>10MΩ)	Very High input impedance(>10000MΩ)
3	Gate is not insulated from channel	Gate is insulated from channel by a layer of Sio_2
4	Channel exists permanently	Channel exists permanently in depletion type but not in enhancement type.
5	Difficult to fabricate than MOSFET	Easier to fabricate
6	Drain resistance is high	Drain resistance is less
7	Gate is formed as a diode	Gate is formed as a capacitor