JFET BIASING

BY

SUDHEER

JFET BIASING

Like BJT, the parameters of FET are also temperature dependent. In FET, as temperature increases drain resistance also increases, reducing the drain current. Thus unlike BJT, thermal runaway does not occur with FET.

The general relationships that can be applied to the d.c. analysis of all FET amplifiers are :

$$I_G = 0 \text{ A} \quad \ldots (1)$$

$$I_D = I_S \quad \ldots (2)$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 \quad \ldots (3)$$

FIXED BIAS

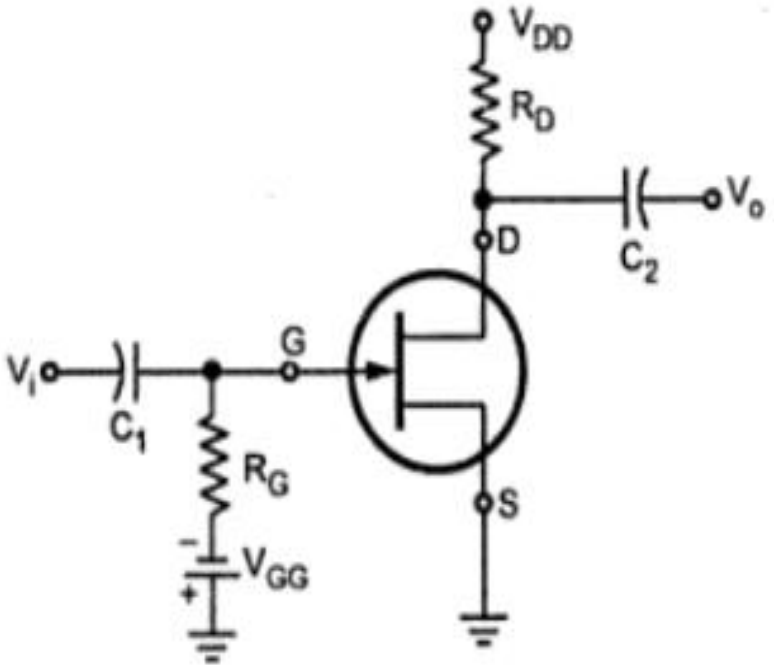


Fig. 3.19 Fixed bias circuit for n-channel circuit

Fig. 3.19 shows the fixed bias circuit for the n-channel JFET. This is the simplest biasing arrangement. To make gate-source junction reverse-biased, a separate supply V_{GG} is connected such that gate is more negative than the source.

D.C. Analysis : For the d.c. analysis coupling capacitors are open circuits. The current through R_G is I_G which is zero. This permits R_G to replace by short circuit equivalent, simplifying the fixed bias circuit as shown in the Fig. 3.19.

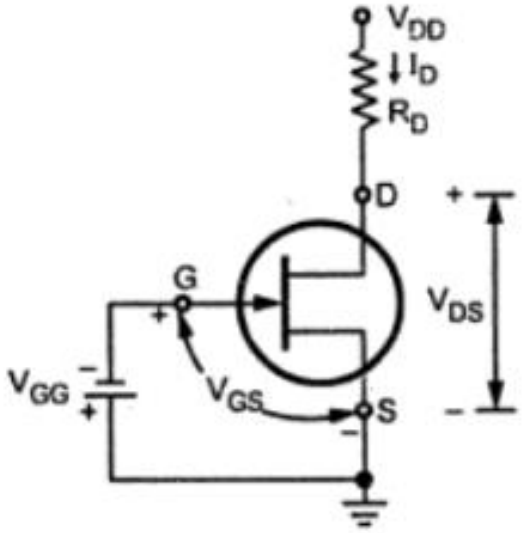


Fig. 3.20 Simplified fixed bias circuit

We know for d.c. analysis

$$I_G = 0 \text{ A}$$

and applying KVL to the input circuit we get,

$$V_{GS} + V_{GG} = 0$$

$$\therefore \quad V_{GS} = -V_{GG} \qquad \ldots (4)$$

Since V_{GG} is a fixed d.c. supply, the voltage V_{GS} is fixed in magnitude, and hence the name fixed bias circuit.

For fixed bias circuit the drain current I_D can be calculated using equation (3).

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_p}\right)^2$$

The drain to source voltage of output circuit can be determined by applying KVL.

$$+ V_{DS} + I_D R_D - V_{DD} = 0$$

$$\therefore V_{DS} = V_{DD} - I_D R_D \quad \ldots (5)$$

The **Q point** of the JFET amplifier with fixed bias circuit is given by :

$$\mathbf{I_{DQ}} = I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]^2$$

$$\mathbf{V_{DSQ}} = V_{DD} - I_{DQ} R_D$$

PROBLEM

Example 3.3 : *For the circuit shown in the Fig. 3.21. Calculate :*

a) V_{GSQ}, *b)* I_{DQ},

c) V_{DSQ}, *d)* V_D

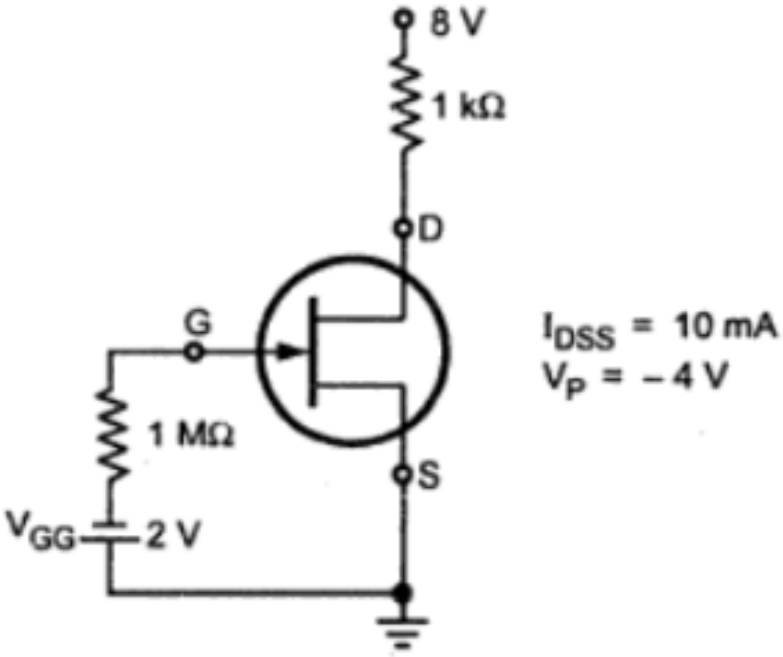


Fig. 3.21

a) $V_{GSQ} = -V_{GG} = -2\ V$

b) $I_{DQ} = I_{DSS}\left(1-\frac{V_{GS}}{V_p}\right)^2 = 10\times10^{-3}\left(1-\frac{-2\ V}{-4\ V}\right)^2$

$= 10\times10^{-3}\ (1-0.5)^2 = 10\times10^{-3}\ (0.25) = 2.5\ mA$

c) $V_{DSQ} = V_{DD} - I_{DQ}R_D = 8\ V - 2.5\times10^{-3}\ (1\times10^3) = 5.5\ V$

d) $V_D = V_{DS} + V_S = 5.5 + 0 = 5.5\ V$

VOLTAGE DIVIDER BIAS CIRCUIT

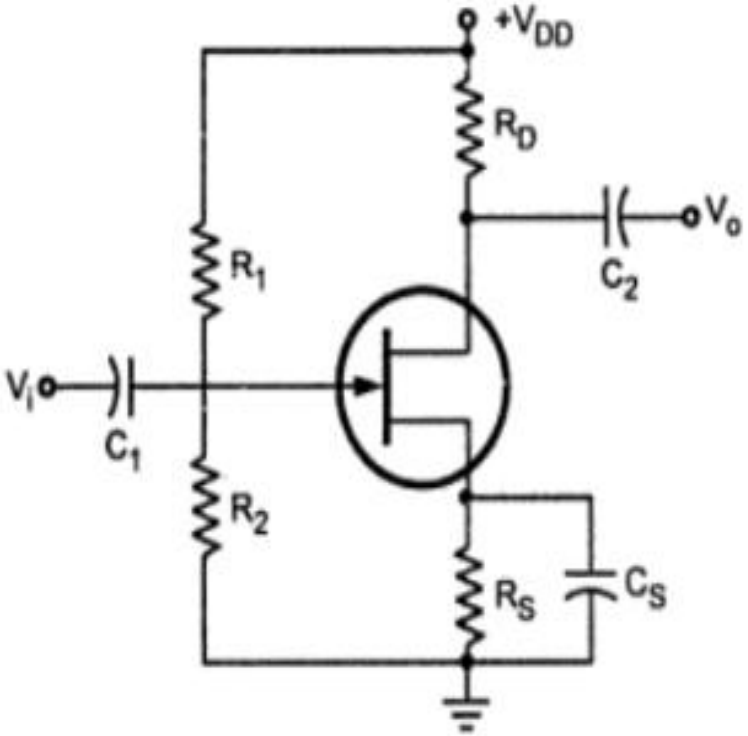


Fig. 3.22 Voltage divider bias for n-channel JFET

The Fig. 3.22 shows n-channel JFET with voltage divider bias. The voltage at the source of the JFET must be more positive than the voltage at the gate in order to keep the gate-source junction reverse-biased. The source voltage is,

$$V_S = I_D R_S$$

The gate voltage is set by resistors R_1 and R_2 as expressed by the following equation using the voltage divider formula :

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD} \qquad \because I_G = 0$$

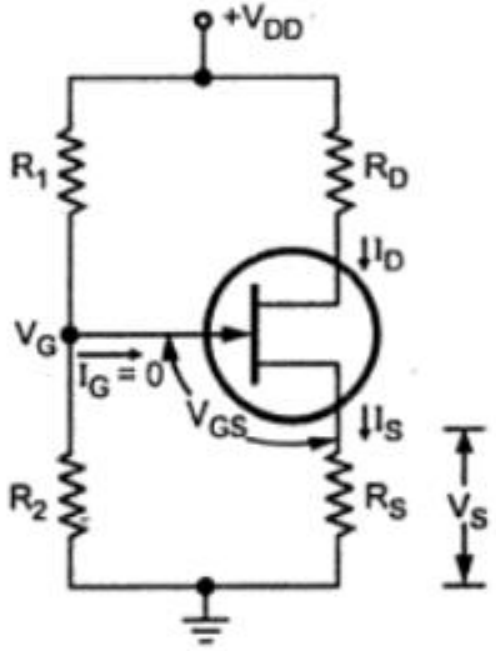


Fig. 3.23 Simplified voltage divider circuit for d.c. analysis

D.C. Analysis :

Applying KVL to the input circuit we get,

$$V_G - V_{GS} - V_S = 0$$

$$\therefore V_{GS} = V_G - V_S = V_G - I_S R_S$$

$$= V_G - I_D R_S \qquad \because I_D = I_S$$

$$\therefore \quad V_{GS} = V_G - I_D R_S \qquad \ldots (6)$$

Applying KVL to the output circuit we get,

$$V_{DS} + I_D R_D + V_S - V_{DD} = 0$$

$$\therefore V_{DS} = V_{DD} - I_D R_D - I_D R_S$$

$$= V_{DD} - I_D (R_D + R_S) \qquad \ldots (7)$$

The Q point of a JFET amplifier using the voltage divider bias is given by :

$$\mathbf{I_{DQ}} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$\mathbf{V_{DSQ}} = V_{DD} - I_D (R_D + R_S)$$

PROBLEM

Example 3.4 : *For circuit shown in Fig. 3.24. Calculate I_D , V_{GS} , V_G, V_{DS} and V_S.*

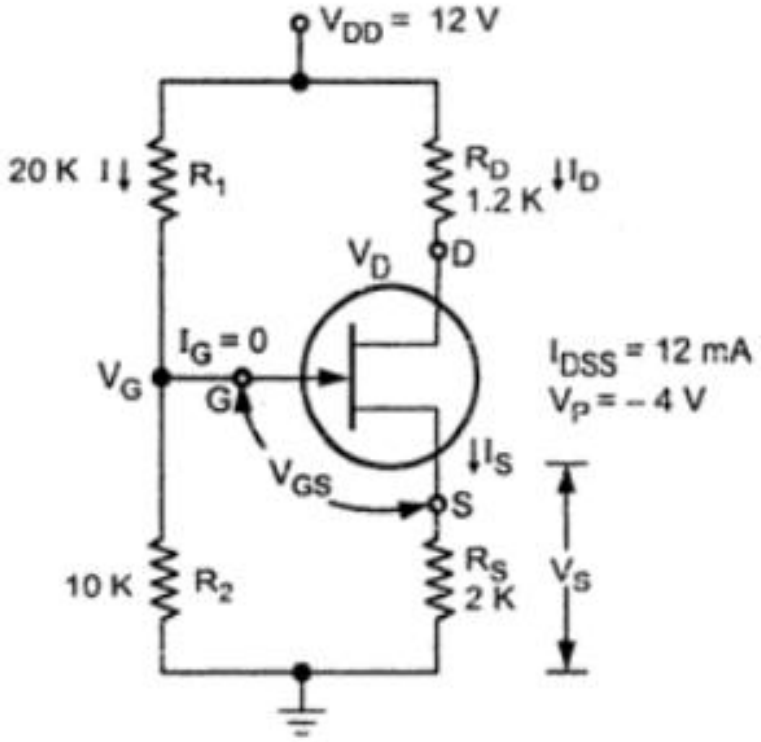


Fig. 3.24

Solution : We have,

$$V_{GS} = V_G - I_D R_S$$

where $$V_G = \frac{V_{DD} R_2}{R_1 + R_2} = \frac{12 \times 10K}{10K + 20K} = 4 \text{ V}$$

$\therefore$ $$V_{GS} = 4 - I_D R_S$$

We have, $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

Substituting value of V_{GS} we get,

$$I_D = I_{DSS}\left(1 - \frac{(4 - I_D R_S)}{V_p}\right)^2 = 12 \times 10^{-3}\left(1 - \frac{(4 - I_D \times 2 \times 10^3)}{-4}\right)^2$$

$$= 12 \times 10^{-3}\,(1 - [\,(-1) + 500 I_D\,])^2 = 12 \times 10^{-3}\,(2 - 500 I_D)^2$$

$$= 12 \times 10^{-3}(4 - 2000 I_D + 250000 I_D^2)$$

$$I_D = (0.048 - 24 I_D + 3000 I_D^2)$$

$\therefore$ $3000 I_D^2 - 25 I_D + 0.048 = 0$

Solving quadratic equation using formula $\frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$ we get,

$$= \frac{-(25) \pm \sqrt{(-25)^2 - 4(3000)(0.048)}}{2(3000)}$$

$$= \frac{25 \pm \sqrt{625 - 576}}{6000} = \frac{25 \pm \sqrt{49}}{6000} = \frac{25 \pm 7}{6000} = 5.33 \text{ mA or } 3 \text{ mA}$$

If we calculate value of V_{DS} taking $I_D = 5.33$ mA we get,

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

$$= 12 - 5.33 \times 10^{-3} (1.2 \text{ K} + 2 \text{ K}) = 12 - 17.07 = -5.07$$

Practically, the value of V_{DS} must be positive, hence $I_D = 5.33$ mA is invalid.

$$\therefore I_D = 3 \text{ mA},$$

$$V_{DS} = 12 - 3 \times 10^{-3} (1.2 \times 10^3 + 2 \times 10^3) = 12 - 9.6 = 2.4 \text{ V}$$

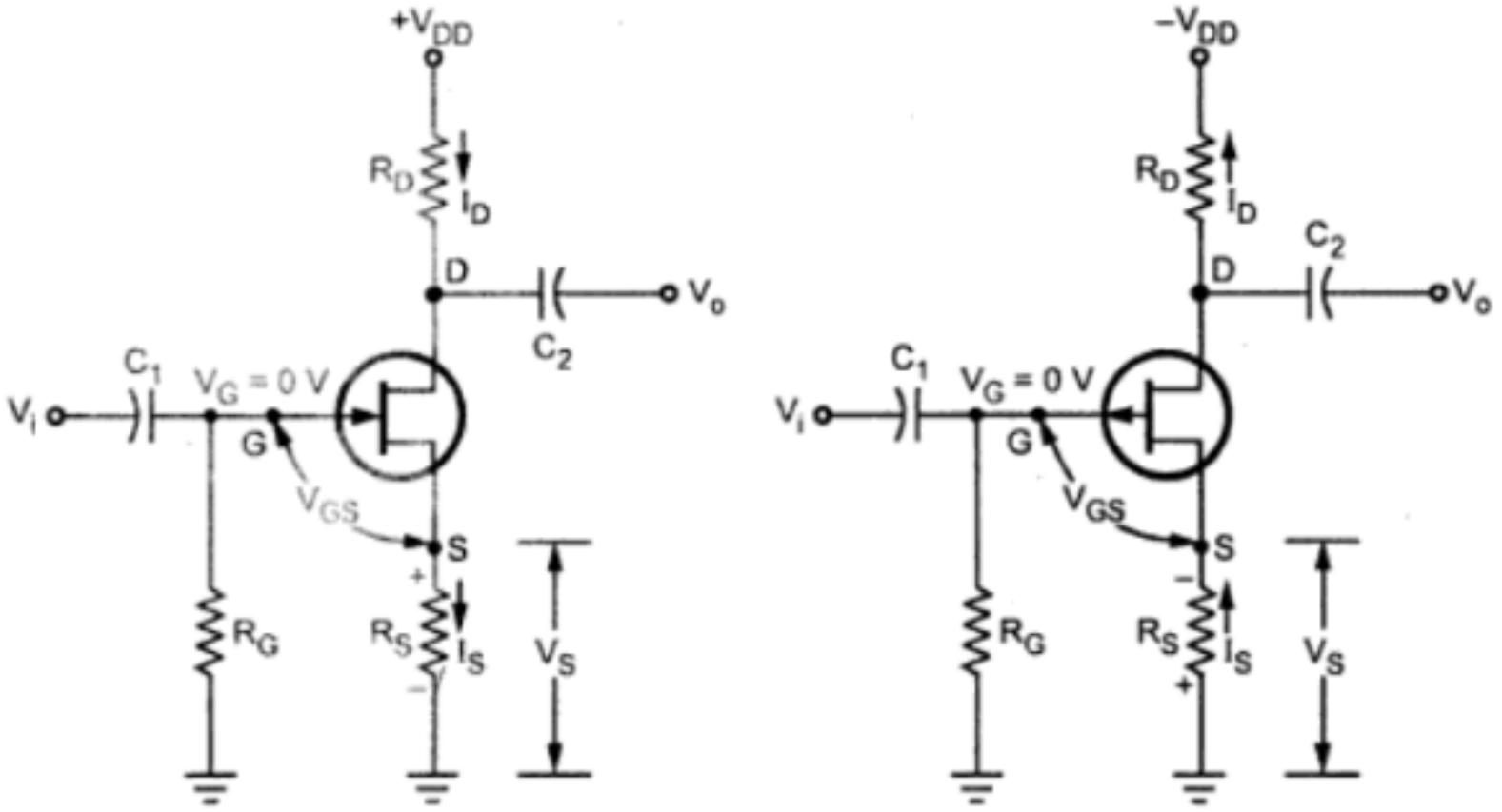
$$\therefore V_{DS} = 2.4 \text{ V}$$

$$V_{GS} = 4 - I_D R_S = 4 - 3 \times 10^{-3} \times 2 \times 10^3 = 4 - 6 = -2 \text{ V}$$

$$V_S = I_D R_S = 3 \times 10^{-3} \times 2 \times 10^3 = 6 \text{ V}$$

SELF BIAS CIRCUIT

Self bias is the most common type of JFET bias. Recall that a JFET must be operated such that the gate source junction is always reverse-biased. This condition requires a negative V_{GS} for an n-channel JFET and a positive V_{GS} for p-channel JFET. This can be achieved using the self bias arrangement shown in Fig. 3.25. The gate resistor, R_G, does not affect the bias because it has essentially no voltage drop across it and therefore the gate remains at 0 V. R_G is necessary only to isolate an a.c. signal from ground in amplifier applications. The voltage drop across resistor, R_S makes gate source junction reverse biased.



Note : $I_S = I_D$ in all JFETs

Fig. 3.25 Self bias circuits for JFET

For the n-channel FET in Fig. 3.25 (a), I_S produces a voltage drop across R_S and makes the source positive with respect to ground. Since $I_S = I_D$ and $V_G = 0$, then

$V_S = I_S R_S = I_D R_S$. The gate to source voltage is,

$$V_{GS} = V_G - V_S = 0 - I_D R_S = - I_D R_S$$

For the p-channel FET in Fig. 3.25 (b), I_S produces a voltage drop across R_S and makes the source negative with respect to ground. Since $I_S = I_D$ and $V_G = 0$, then

$V_S = - I_S R_S = - I_D R_S$. The gate to source voltage is

$$V_{GS} = V_G - V_S = 0 - (- I_D R_S) = + I_D R_S$$

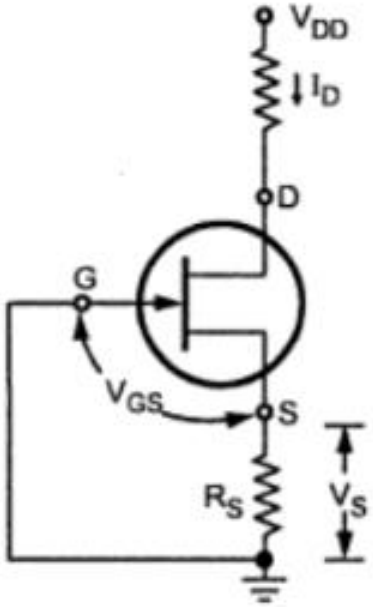


Fig. 3.26 Simplified self bias circuit for dc analysis

In the following D.C. analysis, the n-channel JFET shown in Fig. 3.25 (a) is used to for illustration. For D.C. analysis we can replace coupling capacitors by open circuits and we can also replace the resistor R_G by a short circuit equivalent, since $I_G = 0$. This is illustrated in Fig. 3.26.

We know, equation (3) gives relation between I_D and V_{GS}

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

Substituting value of V_{GS} in above equation we get,

$$I_D = I_{DSS}\left(1 - \frac{-I_D R_S}{V_p}\right)^2 = I_{DSS}\left(1 + \frac{I_D R_S}{V_p}\right)^2 \quad \ldots (8)$$

Applying KVL to the output circuit we get,

$$V_S + V_{DS} + I_D R_D - V_{DD} = 0$$

$$\therefore V_{DS} = V_{DD} - V_S - I_D R_D = V_{DD} - I_D R_S - I_D R_D$$

$$= V_{DD} - I_D (R_S + R_D)$$

$$V_{DS} = V_{DD} - I_D (R_S + R_D) \quad \ldots (9)$$

PROBLEM

Example 3.5 : *For the circuit shown in Fig. 3.27. Calculate* V_{GSQ} , I_{DQ} , V_{DS} , V_S *and* V_D

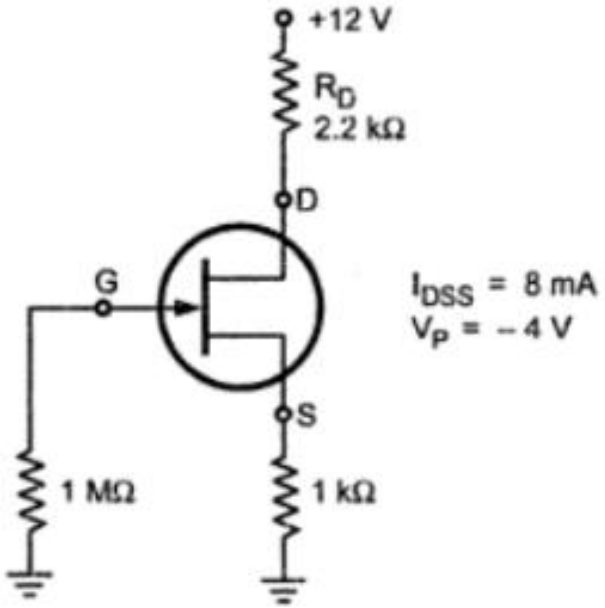


Fig. 3.27

Solution : i) I_D : we have,

$$I_D = I_{DSS}\left(1+\frac{I_D R_S}{V_p}\right)^2$$

$$\therefore \quad I_D = 8\times10^{-3}\left(1+\frac{I_D\times1\times10^3}{-4}\right)^2$$

$$= 8\times10^{-3}\,(1-250\,I_D)^2$$

$$= 8\times10^{-3}\,(1-500\,I_D+62500\,I_D^2)$$

$$I_D = 8\times10^{-3}-4\,I_D+500\,I_D^2$$

$$\therefore \quad 500\,I_D^2-5\,I_D+8\times10^{-3} = 0$$

Solving quadratic equating using formula $\frac{-b\pm\sqrt{b^2-4ac}}{2a}$ we have,

$$= \frac{+5 \pm \sqrt{(-5^2) - 4(500)(8\times10^{-3})}}{2\times(500)}$$

$$= \frac{+5 \pm \sqrt{25-16}}{1000} = \frac{+5 \pm \sqrt{9}}{1000}$$

$$= \frac{+5 \pm 3}{1000} = 8 \text{ mA or } 2 \text{ mA}$$

I_{DQ} cannot have value 8 mA because maximum value of I_D, I_{DSS} is given as 8 mA at $V_{GS} = 0$ and hence I_{DQ} is taken as 2 mA.

ii) $V_{GS_{(Q)}}$: we have,

$$V_{GS_Q} = -I_D R_S = -2\times10^{-3}\times1\times10^{3}$$

$$= -2 \text{ V}$$

iii) $V_{GS} : V_S = I_D R_S = -2\times10^{3}\times1\times10^{3}$

$$= 2 \text{ V}$$

iv) $V_{DS} : V_{DS} = V_{DD} - I_D (R_D + R_S) = 12 - 2\times10^{-3}(2.2\times10^{3} + 1\times10^{3}) = 12 - 6.4$

$$= 5.6 \text{ V}$$

v) $V_D = V_{DS} + V_S = 5.6 + 2 = 7.6 \text{ V}$

Equivalent circuit of FET

Fig. 5.50 shows the small signal low frequency ac equivalent circuit for n-channel JFET. The relation of I_d by V_{gs} is included as a current source $g_m V_{gs}$ connected from drain to source. The input impedance is represented by the open circuit at its input terminals, since gate current I_G is zero. The output impedance is represented by r_d from drain to source.

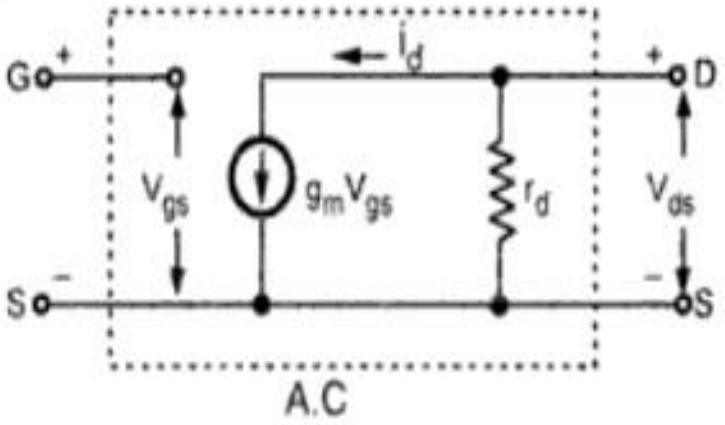


Fig. 5.50 JFET low frequency A.C. equivalent circuit for n-channel JFET

Key Point : *The lower case subscripts represent ac levels.*

Approximate A.C. Equivalent Circuit

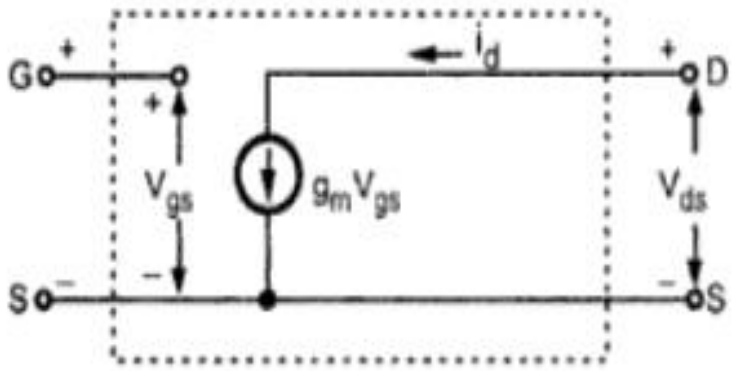


Fig. 5.51 Approximate A.C. equivalent circuit for JFET amplifier

When the value of external drain resistance R_D is very small as compared to the value of output impedance represented by r_d, it is possible to replace r_d by open circuit. This gives us approximate ac equivalent circuit of JFET amplifier, as shown in Fig. 5.51.

CS configuration

In common source amplifier circuit input is applied between gate and source and output is taken from drain and source. In the following sections we see the low frequency equivalent circuits for common source configuration with different biasing techniques.

JFET with fixed bias

Fig. 5.53 shows common source amplifier with fixed bias. The coupling capacitor C_1 and C_2 which are used to isolate the dc biasing from the applied ac signal act as short circuits for the ac analysis.

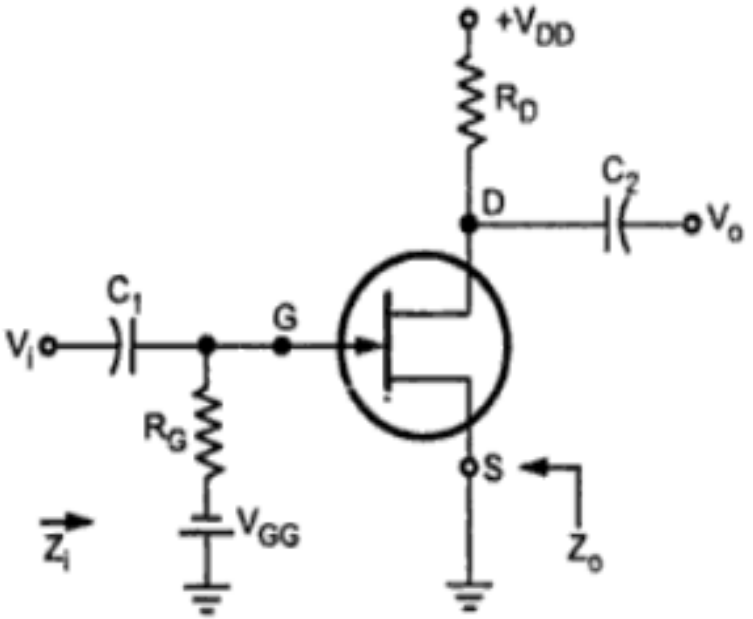


Fig. 5.53 Common source JFET amplifier with fixed bias

Fig. 5.54 shows the low frequency equivalent model for the common source amplifier circuit with fixed bias. It is drawn by replacing :

- All capacitors and dc supply voltages with short circuits and
- JFET with its low frequency equivalent circuit.

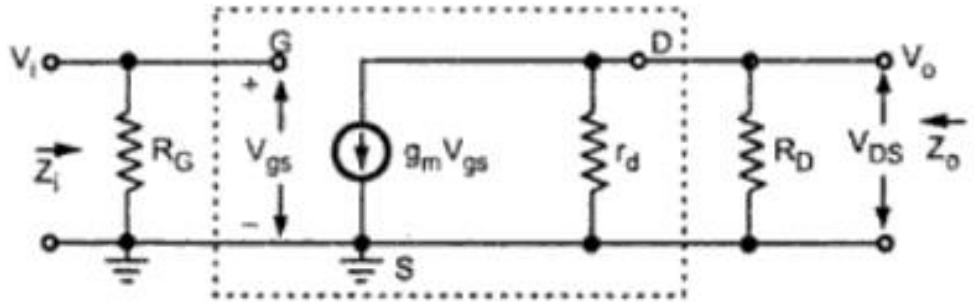


Fig. 5.54 AC equivalent model for the common source amplifier circuit with fixed bias

Now, we see the input impedance output impedance and voltage gain of the above model.

Input impedance Z_i :

Looking into Fig. 5.53 we can say that,

$$Z_i = R_G \quad \ldots (1)$$

Output impedance Z_o :

The output impedance Z_o is the impedance measured looking from the output side with input voltage (V_i) equal to 0. As $V_i = 0$,

$V_{gs} = 0$ and hence $g_m V_{gs} = 0$.

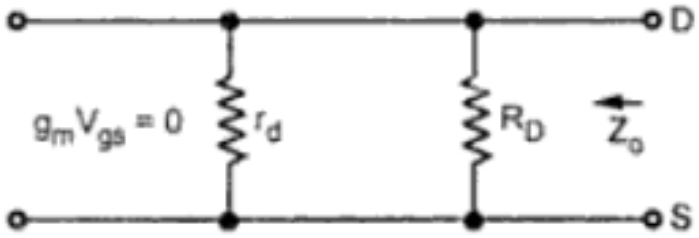


Fig. 5.55

The $g_m V_{gs} = 0$ allows current source to be replaced by an open circuit, as shown in the Fig. 5.54. Therefore the output impedance is

$$Z_o = R_D \,||\, r_d \qquad \ldots (2)$$

If the resistance r_d is sufficiently large compared to R_D, then we say that the output impedance is approximately equal to R_D.

$$Z_o \approx R_D \qquad \because\ r_d >> R_D \qquad \ldots (3)$$

Voltage gain

Voltage gain A_v :

The voltage gain $A_v = \frac{V_{ds}}{V_{gs}} = \frac{V_o}{V_i}$

Looking at Fig. 5.53 we can write

$$V_o = -g_m V_{gs} \ (r_d \,||\, R_D) \quad \ldots (4)$$

As we know $V_i = V_{gs}$ we can write

$$V_o = -g_m V_i \ (r_d \,||\, R_D) \quad \ldots (5)$$

$$\therefore \quad A_v = \frac{V_o}{V_i} = -g_m \ (r_d \,||\, R_D) \quad \ldots (6)$$

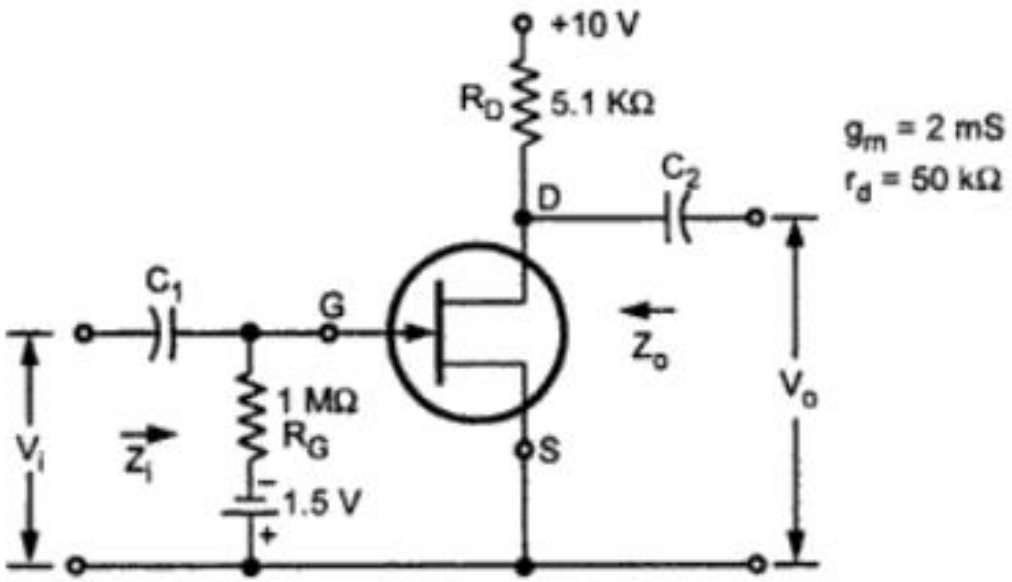
And if $r_d >> R_D$,

$$A_v \approx -g_m R_D \quad \ldots (7)$$

Key Point : *The negative sign in the equation for A_v clearly indicates there is a phase shift of 180° between input and output voltages.*

Problem

Example 5.7 : *For the circuit shown in Fig. 5.56. Determine i) Input impedance ii) Output impedance and iii) Voltage gain.*



i) We have

$$Z_i = R_G = 1\ M\Omega$$

ii) We have

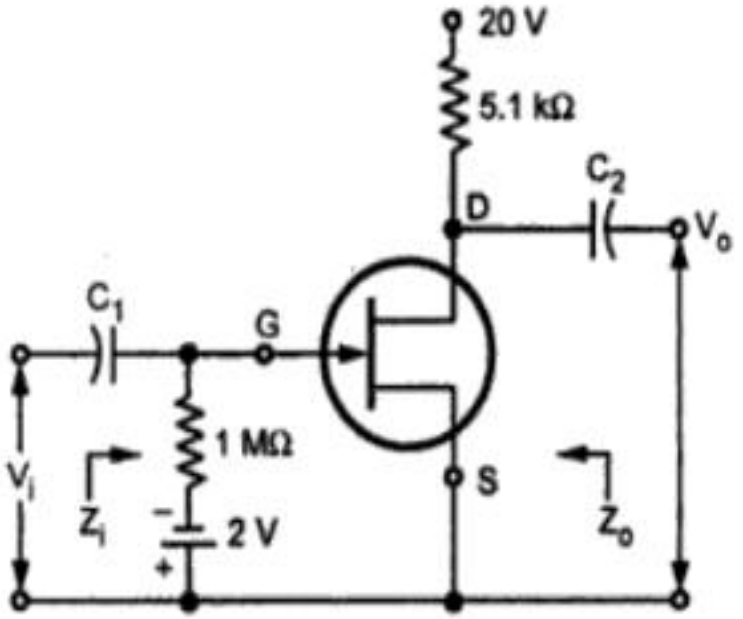
$$Z_o = r_d \,||\, R_D = 50\ K \,||\, 5.1\ K = 4628\ \Omega$$

iii) Voltage gain A_v : We have

$$A_v = -g_m\ (r_d \,||\, R_D) = -2\ mS\ (50\ K \,||\, 5.1\ K) = -2\ mS\ (4628)$$

$$= -9.256$$

Example 5.8 : *For the circuit shown in the Fig. 5.57* $V_{GSQ} = -2$ *V with* $I_{DSS} = 8$ *mA and* $V_p = -8$ *V. Calculate* g_m, r_d, Z_i, Z_o *and* A_v. *The value of* Y_{os} *is given as 20* μ*S.*



i) g_m : We have,

$$g_{mo} = \frac{2 I_{DSS}}{|V_p|} = \frac{2(8\times 10^{-3})}{8V} = 2\ mS$$

Also we have,

$$g_m = g_{mo}\left(1-\frac{V_{GSQ}}{V_p}\right) = 2mS\left(1-\frac{(-2V)}{(-8V)}\right) = 1.5\ mS$$

ii) r_d : $$r_d = \frac{1}{Y_{os}} = \frac{1}{20\ \mu S} = 50\ k\Omega$$

iii) Z_i : We have,

$$Z_i = R_G = 1\ M\Omega$$

iv) $$Z_o = r_d \,||\, R_D$$

v) $$A_v = -g_m\ (r_d \,||\, R_D)$$

JFET with voltage divider bias circuit(Bipassed R_s)

The coupling capacitor C_1 and C_2 which are used to isolate the dc biasing from the applied ac signal act as short circuits for the low frequency analysis. Bypass capacitor C_s also acts as short circuit for the low frequency analysis.

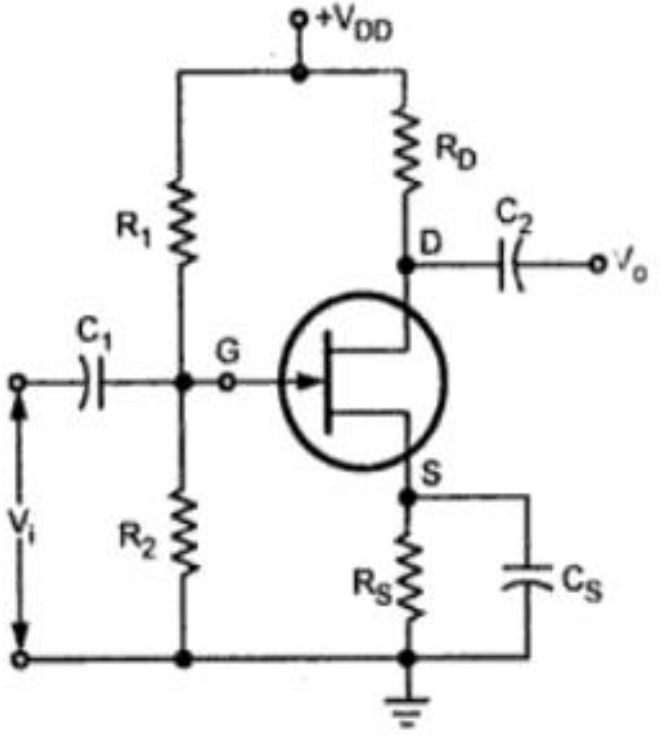
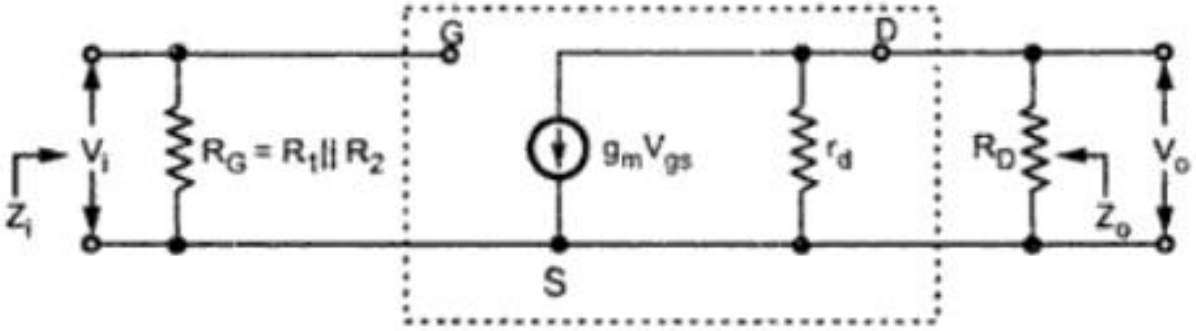


Fig. 5.64 Common source JFET amplifier with voltage divider bias

Fig. 5.64 shows the low frequency equivalent model for the common source amplifier circuit with voltage divider bias. It is drawn by replacing :

- All capacitors and dc supply V_{DD} with short circuits and,
- JFET with its low frequency equivalent circuit



Since the resulting low frequency equivalent circuit is the same as ac equivalent circuit in Fig. 5.59, the equation for Z_i , Z_o and A_v will be the same.

It is important to note that, here,

$$R_G = R_1 \,||\, R_2 \,.$$

$$Z_i = R_G$$

$$= R_1 \,||\, R_2 \qquad \ldots (35)$$

$$Z_o = r_d \,||\, R_D \qquad \ldots (36)$$

If $r_d >> R_D$

$$Z_o \approx R_D \qquad \ldots (37)$$

$$A_v = -g_m (r_d \,||\, R_D) \qquad \ldots (38)$$

If $r_d >> R_D$

$$A_v = -g_m R_D \qquad \ldots (39)$$

CG configuration

In common gate amplifier circuit input is applied between source and gate and output is taken between drain and gate. Fig. 5.74 shows common gate configuration.

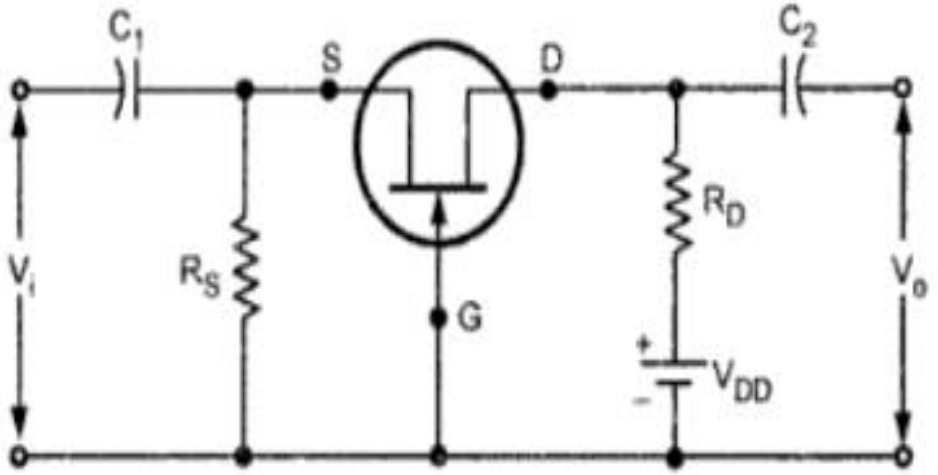


Fig. 5.74 JFET common gate configuration

In common gate configuration, gate voltage is at constant potential. Thus increase in input voltage V_i in positive direction increases the negative gate-source bias voltage. Due to this drain current reduces, reducing the drop I_DR_D. Since $V_D = V_{DD} - I_DR_D$, the reduction in I_D results in an increase in output voltage (V_D). Similarly when input voltage reduces, opposite action takes place which reduces the output voltage. Thus we can say that there is no phase shift between input and output in a common gate amplifier.

Fig. 5.75 shows ac equivalent model for common gate amplifier circuit shown in Fig. 5.74.

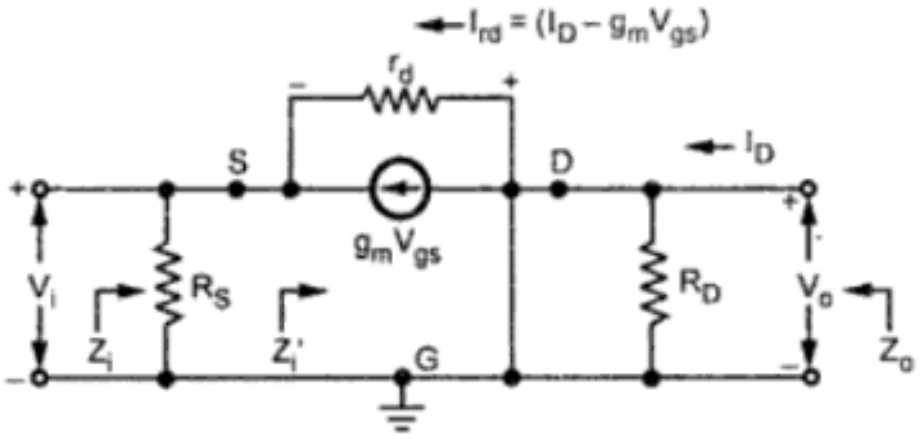


Fig. 5.75 AC equivalent model for common gate amplifier circuit

Input impedance : It is given as,

$$Z_i = R_s \parallel Z_i' \qquad \ldots (1)$$

Let us see the circuit in Fig. 5.76 for determining Z_i'. Z_i' is given by,

$$Z_i' = \frac{V_i}{I}$$

SINCE $I = G_m * V_{gs}$

$V_i = V_{gs}$

If $r_d >> R_D$ and $g_m r_d >> 1$ then we can write,

$$Z_i = R_s \parallel \frac{r_d}{g_m r_d} = R_s \parallel \frac{1}{g_m}$$

Key Point : *Input resistance of CG amplifier is very less as compared to CS and CD amplifiers.*

Output impedance Z_o :

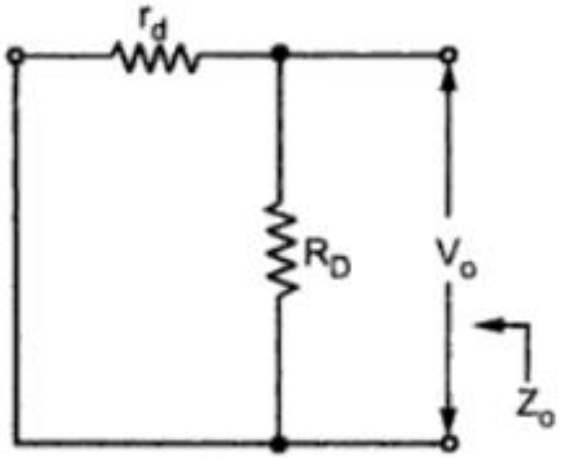


Fig. 5.77

It is the output impedance of the circuit when input is short circuited. Fig. 5.77 shows the ac equivalent model with input short circuited.

As input is short circuited, R_s is also short circuited and V_{gs} becomes = 0 and hence V_{gs} = 0. Look at the Fig. 5.77, Z_o can be given as,

$$Z_o = r_d \parallel R_D \quad \ldots (9)$$

If $r_d >> R_D$,

$$Z_o \approx R_D \quad \ldots (10)$$

Voltage gain A_v, it is given as,

$$A_v = \frac{V_o}{V_i}$$

where $V_o = -I_D R_D$ ... (11)

and $V_i = -V_{gs}$ ... (12)

Applying KVL to the outer loop of Fig. 5.75 we get,

$$V_i + (I_d - g_m V_{gs})\, r_d + I_d R_D = 0 \quad \text{... (13)}$$

As $V_{gs} = -V_i$ we get,

$$V_i + I_d r_d + g_m r_d\, V_i + I_d R_D = 0$$

$$\therefore \quad V_i + g_m r_d V_i = -I_d (r_d + R_D)$$

$$\therefore \quad V_i = \frac{-I_d (r_d + R_D)}{1 + g_m r_d} \quad \text{... (14)}$$

$$\therefore \quad A_v = \frac{V_o}{V_i} = \frac{-I_d + R_D}{\dfrac{-I_d (r_d + R_D)}{1 + g_m r_d}}$$

$$= \frac{R_D(1+g_m r_d)}{r_d + R_D} \qquad \ldots (15)$$

If $r_d >> R_D$ and $g_m r_d >> 1$

$$A_v = \frac{R_D(g_m r_d)}{r_d} = R_D g_m \qquad \ldots (16)$$

Key Point : *From equation (16) we observe that there is no phase shift between input and output in common gate amplifier.*

Example 5.12 : *For common gate amplifier as shown in the Fig. 5.78,* $g_m = 2.8\ mS$, $r_d = 50\ k\Omega$. *Calculate* Z_i, Z_o *and* A_v.

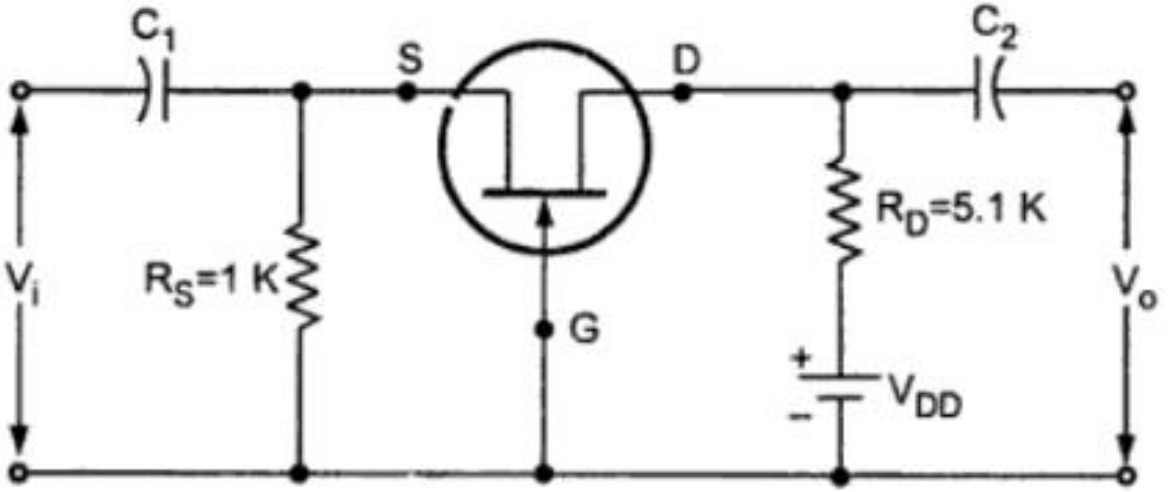


Fig. 5.78

Solution :

i) Z_i : We have,

$$Z_i = R_s \parallel \frac{r_d + R_D}{1 + g_m r_d} = 1\ K \parallel \frac{50\ K + 5.1\ K}{1 + 2.8\ mS \times 50\ K} = 1\ K \parallel 390.8 = 281\ \Omega$$

ii) Z_o : We have,

$$Z_o = r_d \parallel R_D = 50\ K \parallel 5.1\ K$$

iii) A_v : We have

$$A_v = \frac{R_D(1 + g_m r_d)}{r_d + R_D} = \frac{5.1\ K(1 + 2.8\ mS \times 50\ K)}{50\ K + 5.1\ K} = 13.05$$

CD FET AMPLIFIER

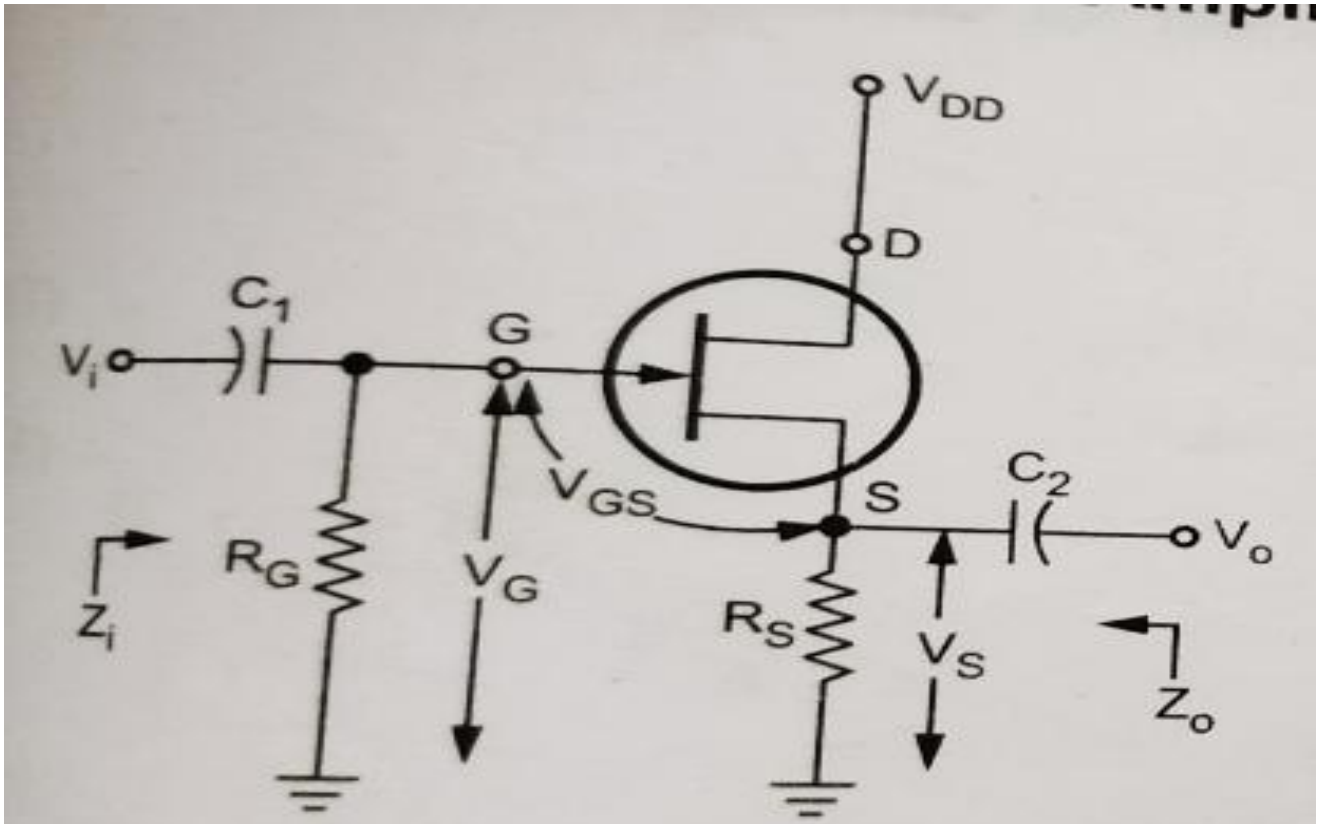


Fig. 7.16 Common drain amplifier circuit

In common drain amplifier circuit input is applied between gate and source and output is taken between source and drain.

Fig. 7.16 shows common drain configuration.

It shows that the output is taken from source and when the d.c. supply is replaced by its short circuit equivalent the drain is grounded and thus common between input and output.

In the common drain circuit the source voltage V_s is given as,

$$V_s = V_G + V_{GS}$$

When a signal is applied to the JFET gate via C_1, V_G varies with the signal. As V_{GS} is fairly constant and $V_s = V_G + V_{GS}$, V_s varies with V_i. For example, if V_i increases by 0.25 V, V_s also approximately increases by 0.25 V. Because the output voltage at the source (V_s) follows changes in the signal voltage applied to the gate, this circuit is also called as source follower.

Fig. 7.17 shows the low frequency equivalent model for the common drain amplifier circuit shown in Fig. 7.16.

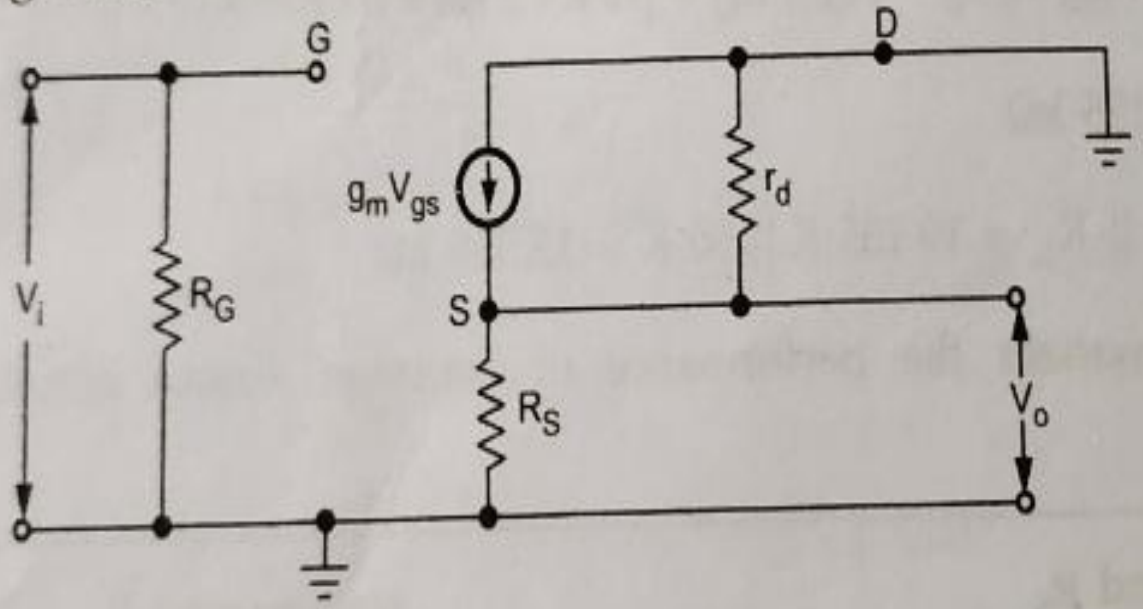


Fig. 7.17 Low frequency equivalent model for common drain circuit

This low frequency equivalent circuit can be simplified as shown in the Fig. 7.17.

INPUT IMPEDANCE

Input Impedance Z_i :

Looking at Fig. 7.18, Z_i can written as,

$$Z_i = R_G \quad \ldots (1$$

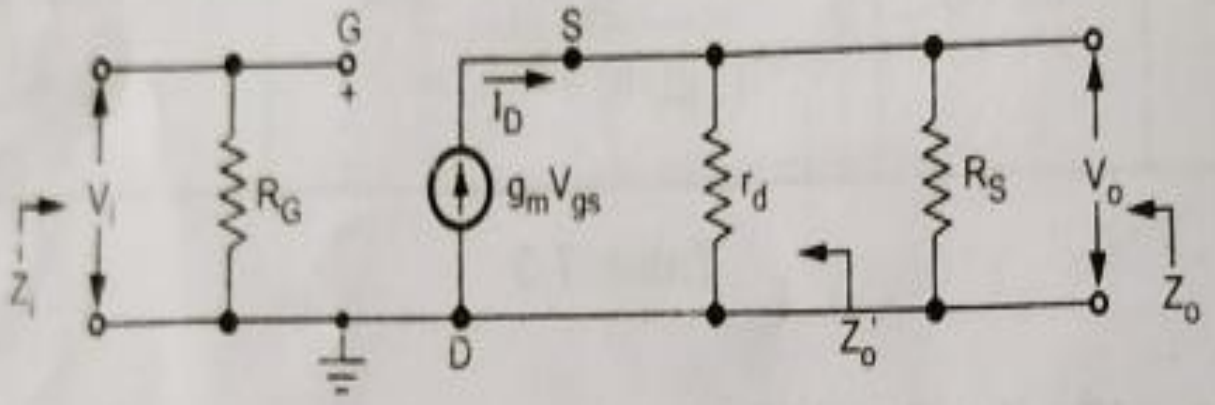


Fig. 7.18 Simplified low frequency equivalent model for common drain circuit

OUTPUT IMPEDANCE

Output Impedance Z_o :

It is given by,

$$Z_o = Z'_o || R_s \quad \ldots (2)$$

where

$$Z'_o = \left.\frac{V_o}{I_d}\right|_{V_i = 0} \quad \ldots (3)$$

Applying KVL to the outer loop we can have,

$$V_i + V_{gs} - V_o = 0 \quad \ldots (4)$$

As

$$V_i = 0,$$

$$V_{gs} = V_o \quad \ldots (5)$$

Looking at Fig. 7.18 we can write that,

$$g_m V_{gs} = I_d \quad \ldots (6)$$

Substituting value of V_{gs} from equation (5) in equation (6) we get,

$$g_m V_o = I_d \quad \ldots (7)$$

$$Z_o' = \frac{V_o}{I_d} = \frac{1}{g_m} \quad \ldots (8)$$

$$\therefore \quad Z_o = \frac{1}{g_m} \| R_s \quad \ldots (9)$$

VOLTAGE GAIN

Voltage Gain A_v :

It is given by,

$$A_v = \frac{V_o}{V_i} \quad \ldots (10)$$

Looking at Fig. 7.18 we can write that,

$$V_o = -I_d\ (r_d \,||\, R_s) \quad \ldots (11)$$

and

$$I_d = g_m\, V_{gs} \quad \ldots (12)$$

$\therefore$

$$V_o = -g_m V_{gs}\ (r_d \,||\, R_s) \quad \ldots (13)$$

Again from equation (4) we have,

$$V_i = -V_{gs} + V_o$$

$$= -V_{gs} + [\,-g_m V_{gs}\ (r_d \,||\, R_s)\,] \quad \ldots (14)$$

$= g_m V_{gs} (r_d \| R_s)]$

Substituting values of V_o and V_i from equations (13) and (14) respectively in above equation (10) we get, ... (14)

$$A_v = \frac{-g_m V_{gs} (r_d \| R_s)}{-V_{gs} (1 + g_m (r_d \| R_s))}$$

$$= \frac{g_m (r_d \| R_s)}{1 + g_m (r_d \| R_s)} \quad \text{... (15)}$$

If $r_d >> R_s$

$$A_v = \frac{g_m R_s}{1 + g_m R_s} \quad \text{... (16)}$$

If $g_m R_s >> 1$

$A_v \approx 1$, but it is always less than one. ... (17)

Key Point :

1. *We observe that the common drain circuit does not provide voltage gain.*
2. *The positive sign in equation (16) also indicates that there is no phase shift between input and output voltages.*

Table 7.4 summarizes the performance of common drain amplifier.

	Exact	$r_d >> R_D$
Z_i	R_G	R_G
Z_o	$\frac{1}{g_m} \parallel R_s$	$\frac{1}{g_m} \parallel R_s$
A_v	$\frac{g_m (r_d \parallel R_s)}{1+g_m (r_d \parallel R_s)}$	$\frac{g_m R_s}{1+g_m R_s}$

PROBLEM

Example 7.5 : *For common drain amplifier as shown in Fig. 7.19,* $g_m = 2.5\ mS$, $r_d = 25\ k\Omega$. *Calculate* Z_i , Z_o *and* A_v .

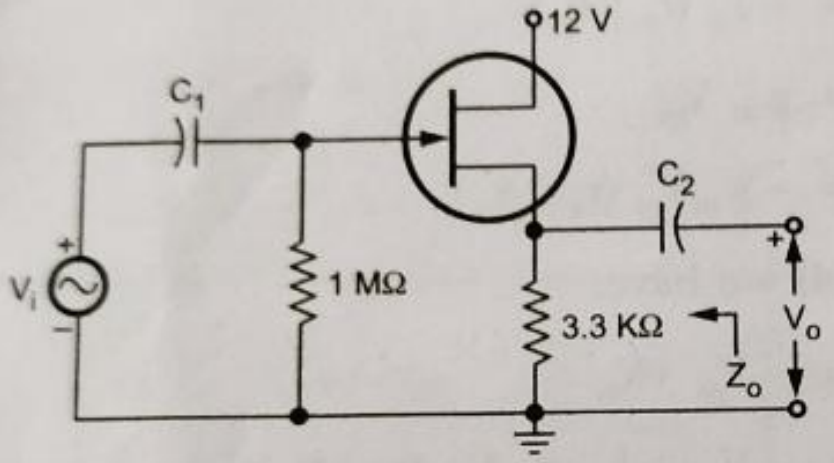


Fig. 7.19

Solution :

Z_i : We have

$$Z_i = R_G = 1\ M\Omega$$

Z_o : We have,

$$Z_o = \frac{1}{g_m} \| R_s = \frac{1}{2.5\ mS} \| 3.3\ K = \frac{400 \times 3.3\ K}{400 + 3.3\ K} = 356.76\ \Omega$$

A_v : We have,

$$A_v = \frac{g_m (r_d \| R_s)}{1 + g_m (r_d \| R_s)} = \frac{2.5\ mS\ (25\ K \| 3.3\ K)}{1 + 2.5\ mS\ (25\ K \| 3.3\ K)}$$

$$= \frac{2.5\ mS\ (2915.2)}{1 + 2.5\ mS\ (2915.2)} = \frac{7.288}{1 + 7.288} = 0.879$$

Feedback Amplifiers

By

Sudheer K

Introduction

Feedback plays an important role in almost all electronic circuits. It is almost invariably used in the amplifier to improve its performance and to make it more ideal. In the process of feedback, a part of output is sampled and fed back to the input of the amplifier. Therefore, at input we have two signals : Input signal, and part of the output which is fed back to the input. Both these signals may be in phase or out of phase. When input signal and part of output signal are in phase, the feedback is called **positive feedback**. On the other hand, when they are in out of phase, the feedback is called **negative feedback**. Use of positive feedback results in oscillations and hence not used in amplifiers.

Classification of amplifiers

Before proceeding with the concepts of feedback, it is useful to understand the classification of amplifiers based on the magnitudes of the input and output impedances of an amplifier relative to the source and load impedances, respectively. The amplifiers can be classified into four broad categories : voltage, current, transconductance and transresistance amplifiers.

Voltage amplifier

Fig. 1.1 shows a Thevenin's equivalent circuit of an amplifier.

If the amplifier input resistance R_i is large compared with the source resistance R_s then $V_i \approx V_s$. If the external load resistance R_L is large compared with the output resistance R_o of the amplifier, then $V_o \approx A_v V_i \approx A_v V_s$. Such amplifier circuit provides a voltage output proportional to the voltage input, and the proportionality factor does not depend on the magnitudes of the source and load resistances. Hence, this amplifier is called **voltage amplifier**. An ideal voltage amplifier must have infinite input resistance R_i and zero output resistance R_o. For practical voltage amplifier we must have $R_i >> R_s$ and $R_L >> R_o$.

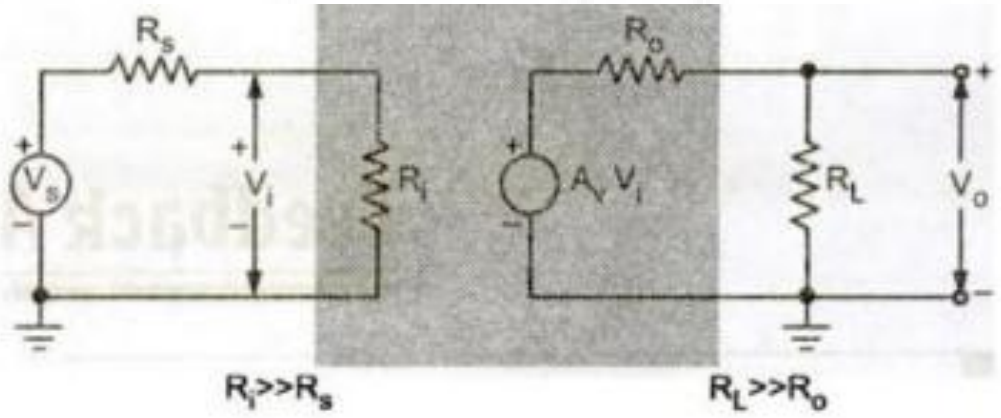


Fig. 1.1 Thevenin's equivalent circuits of a voltage amplifier

Current amplifier

Fig. 1.2 shows Norton's equivalent circuit of a current amplifier. If amplifier input resistance $R_i \to 0$, then $I_i \approx I_s$. If amplifier output resistance $R_o \to \infty$, then $I_L = A_i I_i$. Such amplifier provides a current output proportional to the signal current, and the proportionality factor is independent of source and load resistances. This amplifier is called **current amplifier**. An ideal current amplifier must have zero input resistance R_i and infinite output resistance R_o. For practical current amplifier we must have $R_i \ll R_s$ and $R_o \gg R_L$.

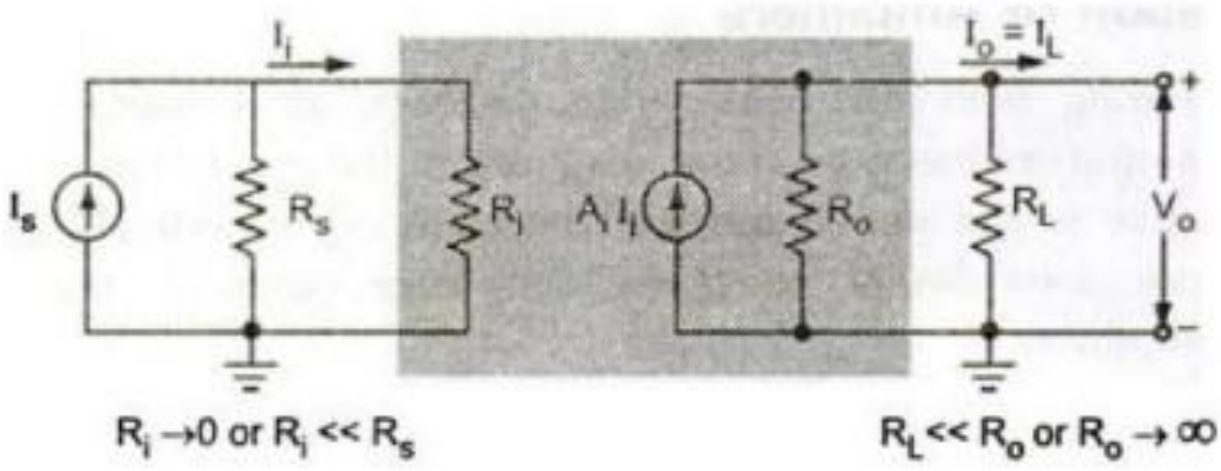


Fig. 1.2 Norton's equivalent circuits of a current amplifier

Transconductance amplifier

Fig. 1.3 shows a transconductance amplifier with a Thevenin's equivalent in its input circuit and Norton's equivalent in its output circuit. In this amplifier, an output current is proportional to the input signal voltage and the proportionality factor is independent of the magnitudes of the source and load resistances. Ideally, this amplifier must have an infinite input resistance R_i and infinite output resistance R_o. For practical transconductance amplifier we must have $R_i >> R_s$ and $R_o >> R_L$.

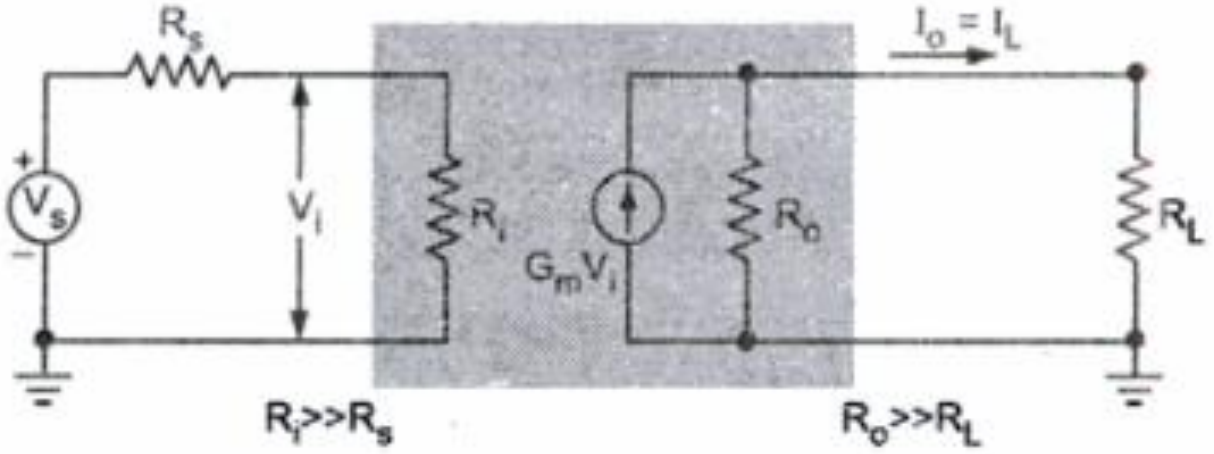


Fig. 1.3 Transconductance amplifier

Transresistance amplifier

Fig. 1.4 shows a transresistance amplifier with a Norton's equivalent in its input circuit and a Thevenin's equivalent in its output circuit. In this amplifier an output voltage is proportional to the input signal current and the proportionality factor is independent on the source and load resistances. Ideally, this amplifier must have zero input resistance R_i and zero output resistance R_o. For practical transresistance amplifier we must have $R_i \ll R_s$ and $R_o \ll R_L$.

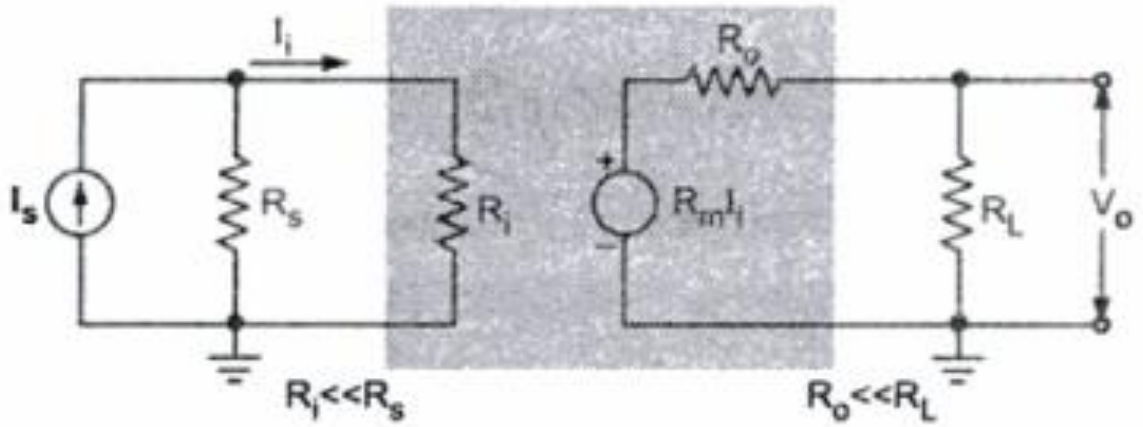


Fig. 1.4

Block diagram of negative feedback amplifier

In the previous section we have seen four basic amplifier types and their ideal characteristics. In each one of these circuits we can sample the output voltage or current by means of a suitable sampling network and apply this signal to the input through a feedback two port network, as shown in the Fig. 1.5. At the input the feedback signal is combined with the input signal through a mixer network and is fed into the amplifier.

As shown in the Fig. 1.5 feedback connection has three networks :

- Sampling Network
- Feedback Network
- Mixer Network

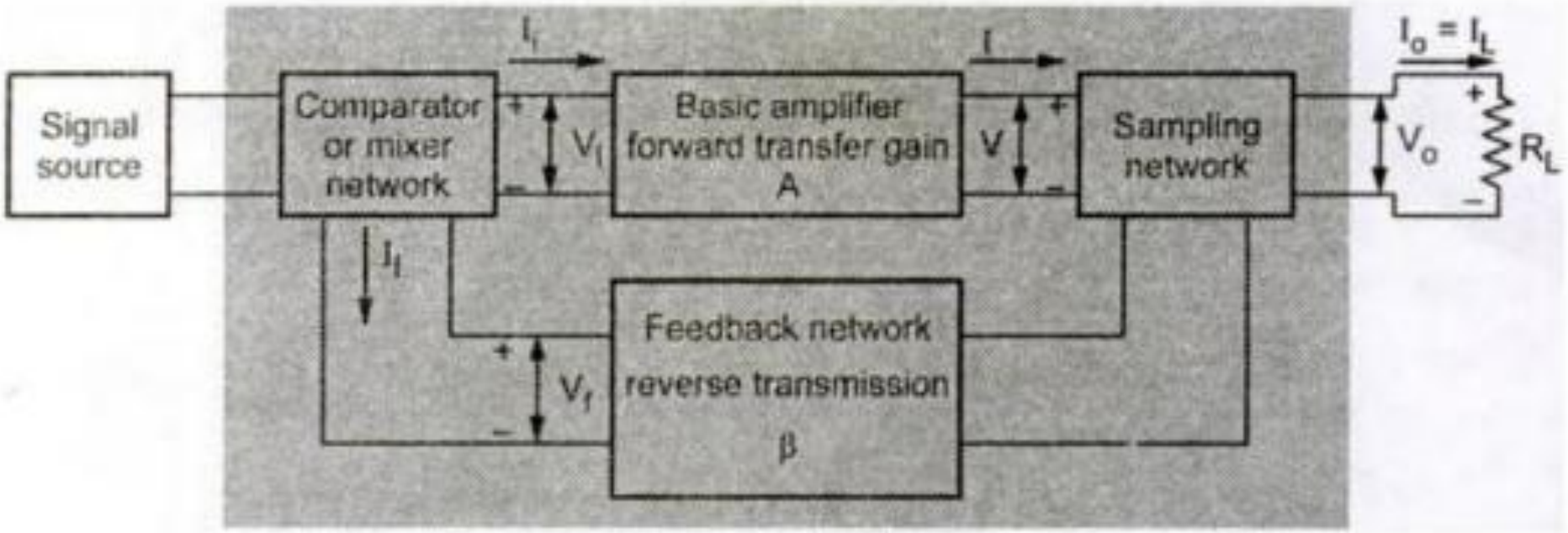
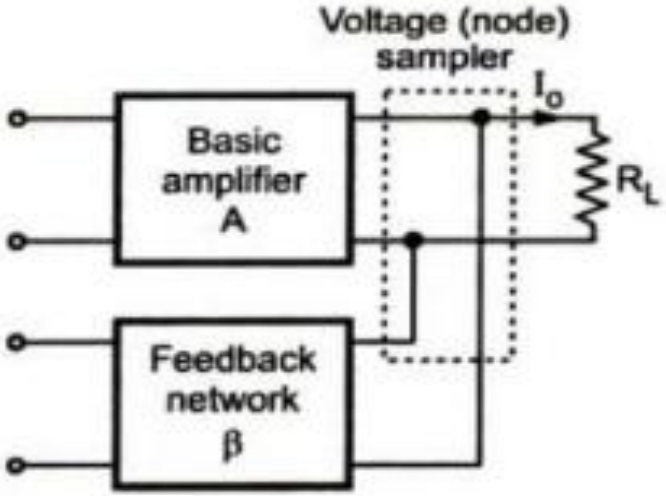


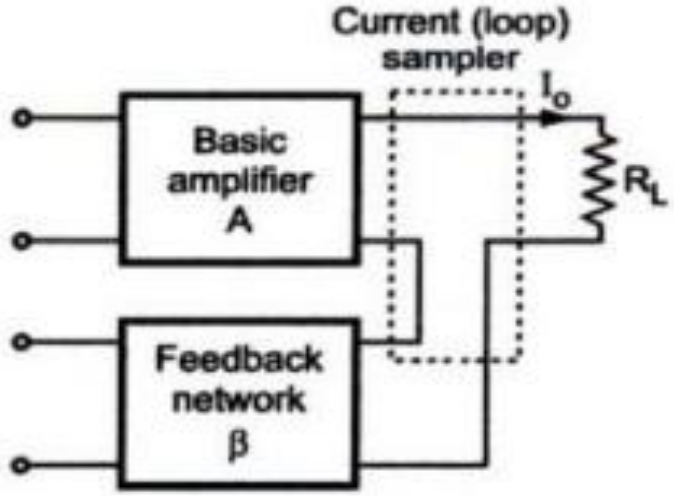
Fig. 1.5 Block diagram of amplifier with feedback

Sampling Network

There are two ways to sample the output, according to the sampling parameter, either voltage or current. The output voltage is sampled by connecting the feedback network in shunt across the output, as shown in the Fig. 1.6 (a). This type of connection is referred to as voltage, or node, sampling. The output current is sampled by connecting the feedback network in series with the output as shown in the Fig. 1.6 (b). This type of connection is referred to as current, or loop, sampling.



(a) Voltage or node sampling



(b) Current or loop sampling

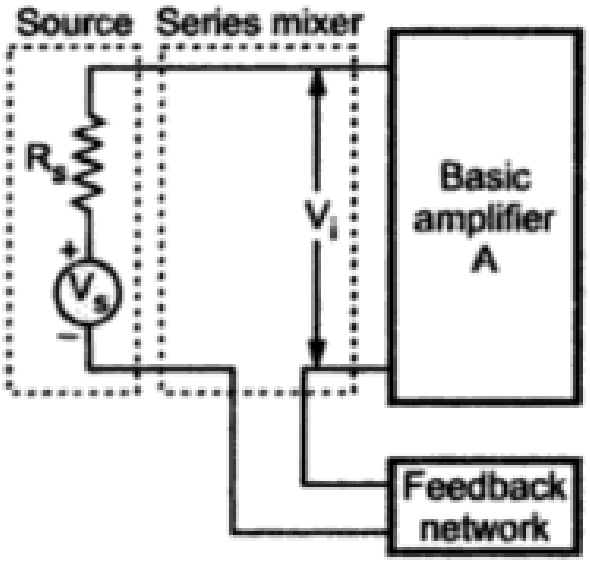
It may consists of resistors, capacitors, and inductors. Most often it is simply a resistive configuration. It provides reduced portion of the output as feedback signal to the input mixer network. It is given as

$$V_f = \beta V_o$$

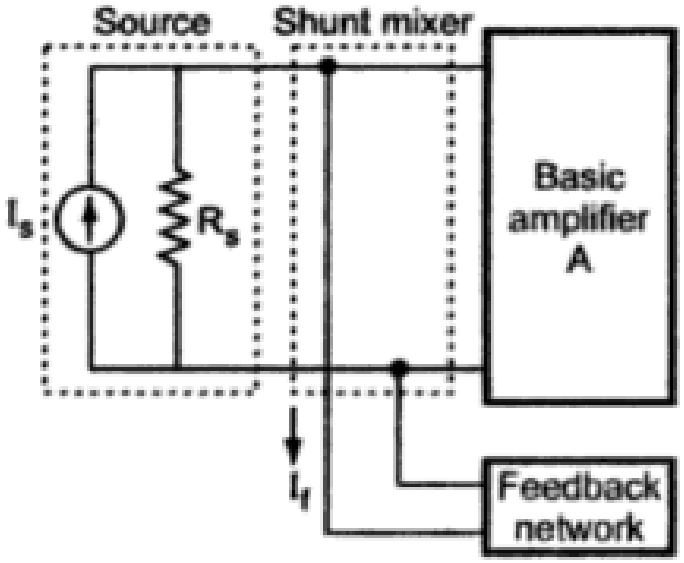
where β is a **feedback factor** or **feedback ratio**. The symbol β used in feedback circuits represents feedback factor which always lies between 0 and 1. It is totally different from β symbol used to represent current gain in common emitter amplifier, which is greater than 1.

Mixer Network

Like sampling, there are two ways of mixing feedback signal with the input signal. These are : series input connection and shunt input connection. The Fig. 1.7 (a) and (b) show the simple and very common **series (loop)** input and **shunt (node)** input connections, respectively.



(a) Series mixing



(b) Shunt mixing

Transfer Ratio (Gain)

In Fig. 1.5, the ratio of the output signal to the input signal of the basic amplifier is represented by the symbol A. The suffix of A given next, represents the different transfer ratios.

$$\frac{V}{V_i} = A_v = \text{Voltage gain} \quad \ldots (1)$$

$$\frac{I}{I_i} = A_i = \text{Current gain} \quad \ldots (2)$$

$$\frac{I}{V_i} = G_m = \text{Transconductance} \quad \ldots (3)$$

$$\frac{V}{I_i} = R_m = \text{Transresistance} \quad \ldots (4)$$

The transfer gain with feedback is represented by the symbol A_f. It is defined as the ratio of the output signal to the input signal of the amplifier configuration shown in Fig. 1.5. Hence A_f is used to represent any one of the following four ratios :

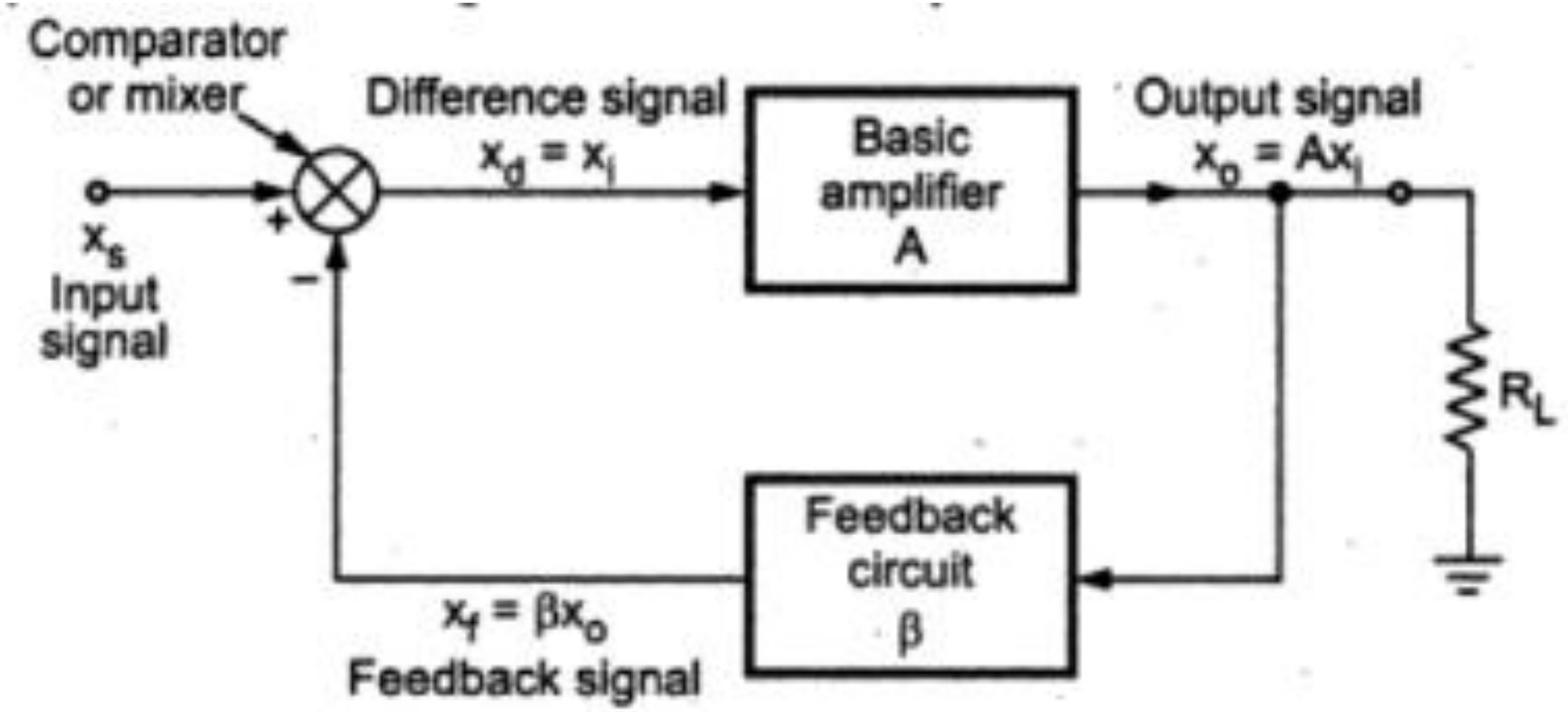
$$\frac{V_o}{V_s} = A_{Vf} = \text{Voltage gain with feedback} \quad \ldots (5)$$

$$\frac{I_o}{I_s} = A_{If} = \text{Current gain with feedback} \quad \ldots (6)$$

$$\frac{I_o}{V_s} = G_{Mf} = \text{Transconductance with feedback} \quad \ldots (7)$$

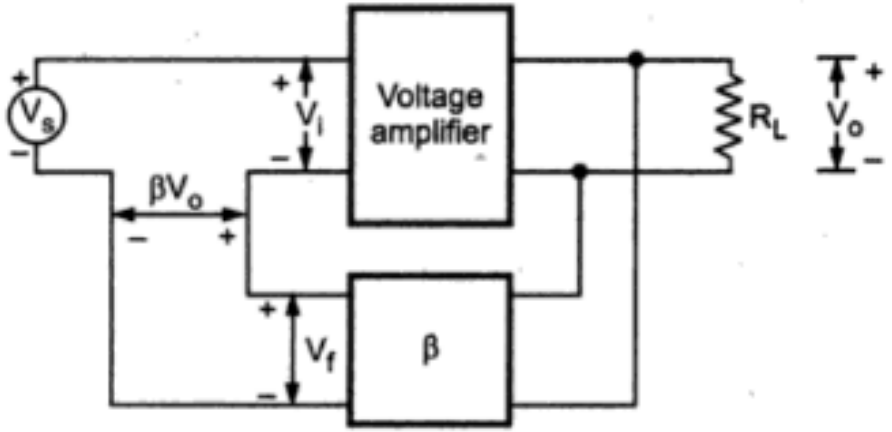
$$\frac{V_o}{I_s} = R_{Mf} = \text{Transresistance with feedback} \quad \ldots (8)$$

Negative feed back Amplifier

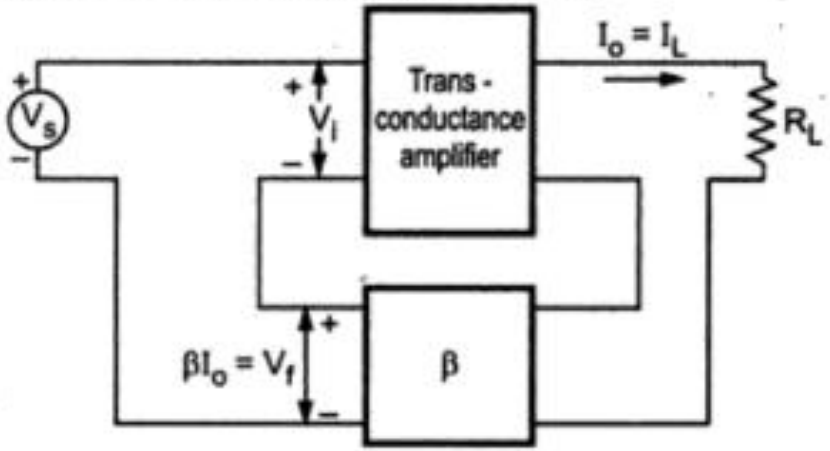


-ve feedback in Amplifiers

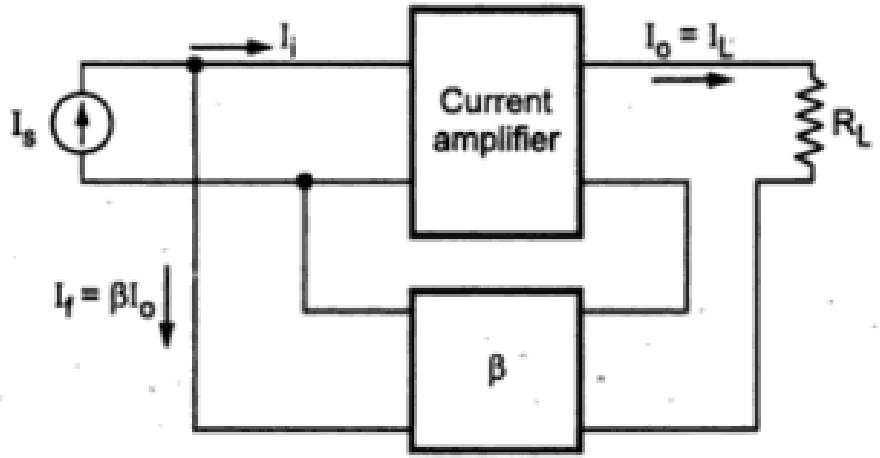
Voltage amplifier with voltage series feedback



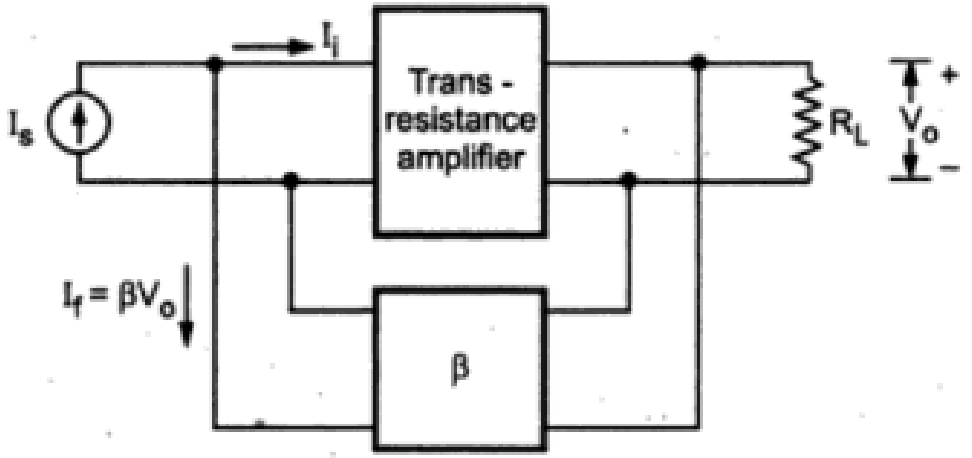
Transconductance amplifier with current series feedback



Current amplifier with current-shunt feedback



Transresistance amplifier with voltage shunt feedback



Effect of –ve feedback on Gain

We have seen, the symbol A is used to represent transfer gain of the basic amplifier without feedback and symbol A_f is used to represent transfer gain of the basic amplifier with feedback. These are given as

$$A = \frac{X_o}{X_i} \text{ and } A_f = \frac{X_o}{X_s}$$

where

X_o = Output voltage or output current

X_i = Input voltage or input current

X_s = Source voltage or source current

As it is a negative feedback the relation between X_i and X_s is given as

$$X_i = X_s + (-X_f)$$

where

X_f = Feedback voltage or feedback current

$$\therefore \quad A_f = \frac{X_o}{X_s} = \frac{X_o}{X_i + X_f}$$

Dividing by X_i to numerator and denominator we get,

$$A_f = \frac{X_o / X_i}{(X_i + X_f) / X_i}$$

$$= \frac{A}{1 + X_f / X_i} \quad \because A = \frac{X_o}{X_i}$$

$$= \frac{A}{1 + (X_f / X_o)(X_o / X_i)}$$

$$\therefore \quad A_f = \frac{A}{1 + \beta A} \quad \because \beta = \frac{X_f}{X_o} \qquad \ldots (1)$$

where β is a feedback factor

Looking at equation we can say that gain without feedback (A) is always greater than gain with feedback ($A/(1 + \beta A)$) and it decreases with increase in β i.e. increase in feedback factor.

For voltage amplifier, gain with negative feedback is given as

$$A_{vf} = \frac{A_v}{1 + A_v \beta} \quad \ldots (2)$$

where A_v = Open loop gain i.e. gain without feedback

β = Feedback factor

Stability of Gain

The transfer gain of the amplifier is not constant as it depends on the factors such as operating point, temperature, etc. This lack of stability in amplifiers can be reduced by introducing negative feedback.

We know that,

$$A_f = \frac{A}{1+\beta A}$$

Differentiating both sides with respect to A we get,

$$\frac{dA_f}{dA} = \frac{(1+\beta A)1-\beta A}{(1+\beta A)^2}$$

$$= \frac{1}{(1+\beta A)^2}$$

$$\therefore \quad dA_f = \frac{dA}{(1+\beta A)^2}$$

Dividing both sides by A_f we get,

$$\frac{dA_f}{A_f} = \frac{dA}{(1+\beta A)^2} \times \frac{1}{A_f}$$

$$= \frac{dA}{(1+\beta A)^2} \times \frac{(1+\beta A)}{A_f} \qquad \text{since } A_f = \frac{A}{1+\beta A}$$

$$\frac{dA_f}{A_f} = \frac{dA}{A} \frac{1}{(1+\beta A)} \qquad \ldots (3)$$

where

$\frac{dA_f}{A_f}$ = Fractional change in amplification with feedback

$\frac{dA}{A}$ = Fractional change in amplification without feedback

Looking at equation (3) we can say that change in the gain with feedback is less than the change in gain without feedback by factor $(1+\beta A)$. The fractional change in amplification with feedback divided by the fractional change without feedback is called the **sensitivity of the transfer gain** $(1/\ (1/(1+\beta A))$. The reciprocal of the sensitivity is called the **desensitivity D** $(1+\beta A)$.

Frequency response & Bandwidth

We know that,

$$A_f = \frac{A}{1+\beta A}$$

Using this equation we can write,

$$A_{f\,mid} = \frac{A_{mid}}{1+\beta A_{mid}} \quad \ldots (9)$$

$$A_{f\,low} = \frac{A_{low}}{1+\beta A_{low}} \quad \ldots (10)$$

and

$$A_{f\ high} = \frac{A_{high}}{1+\beta A_{high}} \quad \ldots (11)$$

Now we analyse the effect of negative feedback on lower cutoff and upper cutoff frequency of the amplifier.

Lower cutoff frequency

We know that, the relation between gain at low frequency and gain at mid frequency, is given as,

$$\frac{A_{low}}{A_{mid}} = \frac{1}{1-j\left(\frac{f_L}{f}\right)} \quad \therefore A_{low} = \frac{A_{mid}}{1-j\left(\frac{f_L}{f}\right)} \qquad \ldots (12)$$

Substituting value of A_{low} in equation 7.18 we get,

$$A_{f\,low} = \frac{\frac{A_{mid}}{1-j\left(\frac{f_L}{f}\right)}}{1+\beta\left(\frac{A_{mid}}{1-j\left(\frac{f_L}{f}\right)}\right)}$$

$$= \frac{A_{mid}}{1-j\left(\frac{f_L}{f}\right)+A_{mid}\,\beta}$$

$$= \frac{A_{mid}}{(1+A_{mid}\beta)-j\left(\frac{f_L}{f}\right)}$$

Dividing numerator and denominator by $(1 + A_{mid}\,\beta)$ we get,

$$A_{f\,low} = \frac{\dfrac{A_{mid}}{1+A_{mid}\beta}}{1-j\left[\dfrac{f_L}{\dfrac{1+A_{mid}\beta}{f}}\right]}$$

$$= \frac{A_{f\,mid}}{1-j\left[\left(\dfrac{f_L}{\dfrac{1+A_{mid}\,\beta}{f}}\right)\right]} \quad \because A_f\ mid = \frac{A_{mid}}{1+A_{mid}\,\beta}$$

$$\therefore \quad \frac{A_{f\,low}}{A_{f\,mid}} = \frac{1}{1-j\left(\dfrac{f_{Lf}}{f}\right)} \qquad \ldots(13)$$

where

Lower cutoff frequency with feedback = $f_{Lf} = \dfrac{f_L}{1+A_{mid}\,\beta}$ ... (14)

From equation (14), we can say that lower cutoff frequency with feedback is less than lower cutoff frequency without feedback by factor $(1+A_{mid}\,\beta)$. Therefore, by introducing negative feedback low frequency response of the amplifier is improved.

Upper Cutoff Frequency

We know that, the relation between gain at high frequency and gain at mid frequency is given as,

$$\frac{A_{high}}{A_{mid}} = \frac{1}{1-j\left(\frac{f}{f_H}\right)}$$

$$\therefore \quad A_{high} = \frac{A_{mid}}{1-j\left(\frac{f}{f_H}\right)} \qquad \ldots (15)$$

Substituting value of A_{high} in equation (11) we get,

$$A_{f\,high} = \frac{\dfrac{A_{mid}}{1-j\left(\dfrac{f}{f_H}\right)}}{1+\beta\left(\dfrac{A_{mid}}{1-j\left(\dfrac{f}{f_H}\right)}\right)} = \frac{A_{mid}}{1-j\left(\dfrac{f}{f_H}\right)+A_{mid}\beta}$$

Dividing numerator and denominator by $(1 + A_{mid}\,\beta)$ we get,

$$A_{f\,high} = \frac{\dfrac{A_{mid}}{1+A_{mid}\,\beta}}{1-j\left[\dfrac{f}{(1+A_{mid}\beta)\,f_H}\right]}$$

$$A_{f\,high} = \frac{A_{f\,mid}}{1-j\left[\dfrac{f}{(1+A_{mid}\beta)\,f_H}\right]} \quad \because\ A_{f\,mid} = \frac{A_{mid}}{1+A_{mid}\beta}$$

$$= \frac{A_{f\,mid}}{1-j\left(\dfrac{f}{f_{Hf}}\right)}$$

$$f_{Hf} = (1 + A_{mid}\,\beta)\, f_H \qquad \ldots (16)$$

From equation (16, we can say that upper cutoff frequency with feedback is greater than upper cutoff frequency without feedback by factor $(1 + A_{mid}\,\beta)$. Therefore, by introducing negative feedback high frequency response of the amplifier is improved.

Bandwidth

Bandwidth

The bandwidth of the amplifier is given as

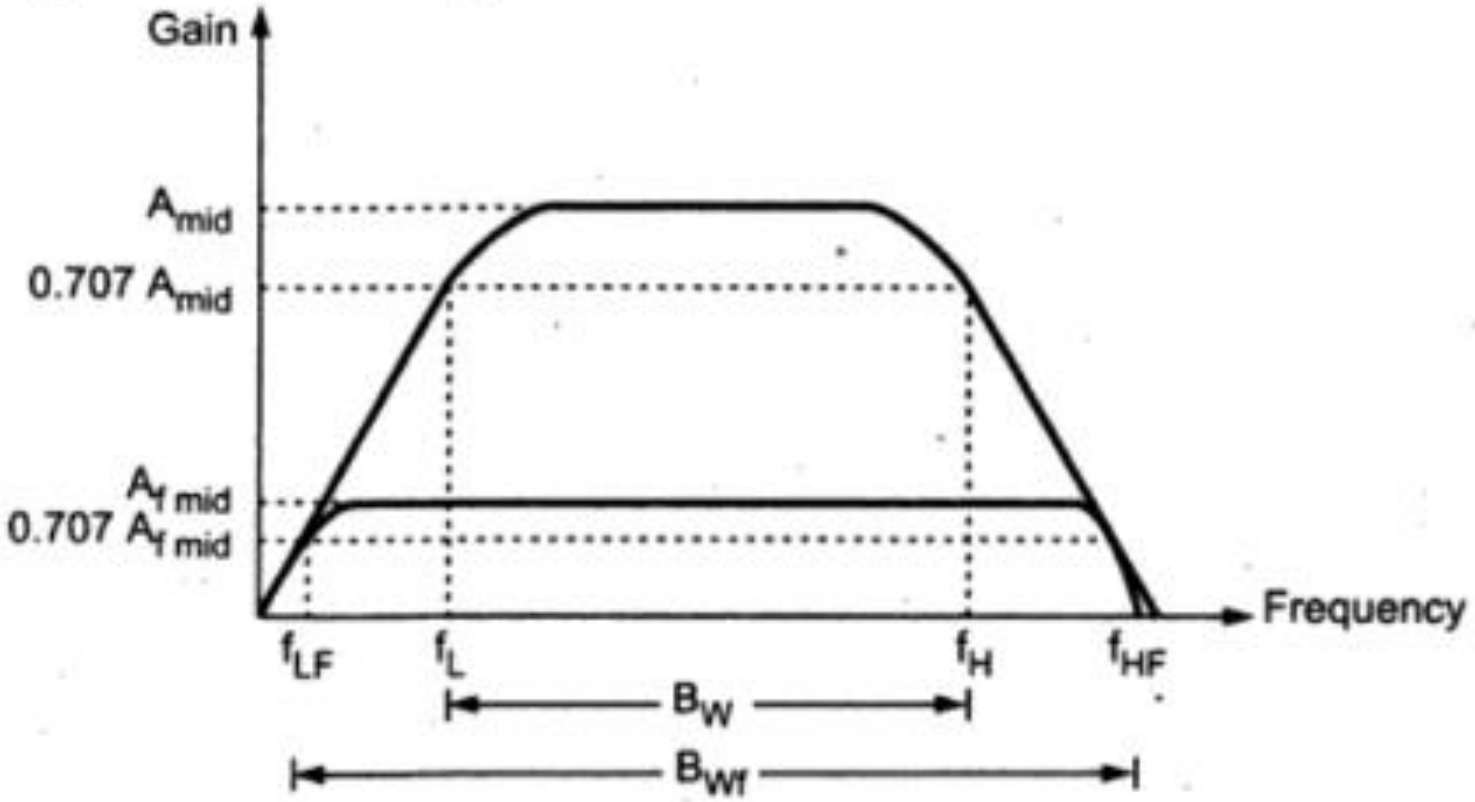
$$BW = \text{Upper cutoff frequency} - \text{lower cutoff frequency}$$

$\therefore$ Bandwidth of the amplifier with feedback is given as

$$BW_f = f_{Hf} - f_{Lf} = (1 + A_{mid}\,\beta)\, f_H - \frac{f_L}{(1 + A_{mid}\,\beta)} \qquad \ldots (17)$$

It is very clear that $(f_{Hf} - f_{Lf}) > (f_H - f_L)$ and hence bandwidth of amplifier with feedback is greater than bandwidth of amplifier without feedback, as shown in Fig. 7.10.

Effect of negative feedback on gain and bandwidth



Frequency Distortion

If $\beta A >> 1$, then

$$A_f = \frac{A}{1+\beta A} = \frac{A}{\beta A}$$

$$= \frac{1}{\beta}$$

From equation (8) we can say that if the feedback network does not contain reactive elements, the overall gain is not a function of frequency. Under such conditions frequency and phase distortion is substantially reduced.

If β is made up of reactive components, the reactances of these components will change with frequency, changing the β. As a result, gain will also change with frequency. This fact is used in tuned amplifiers. In tuned amplifiers, feedback network is designed such that at tuned frequency $\beta \to 0$ and at other frequencies $\beta \to \infty$. As a result, amplifier provides high gain for signal at tuned frequency and relatively reject all other frequencies.

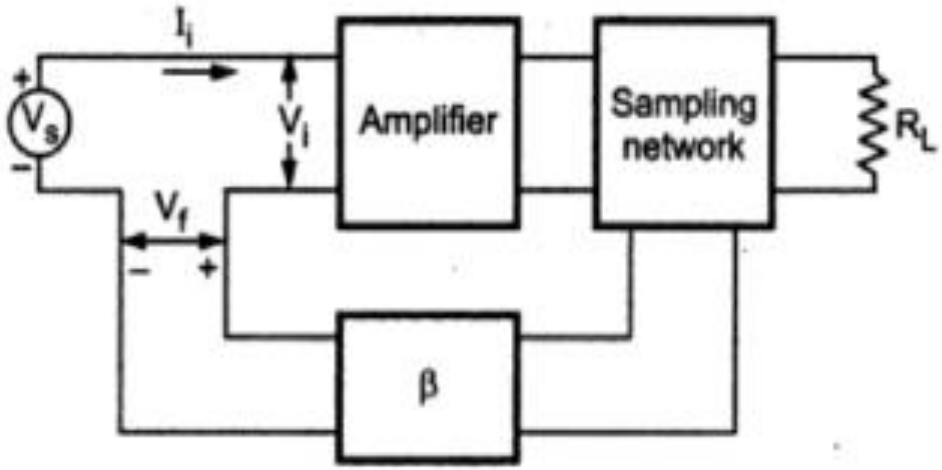
Noise

Signal feedback reduces the amount of noise signal and non linear distortion. The factor $(1 + \beta A)$ reduces both input noise and resulting nonlinear distortion for considerable improvement. Thus, noise and non linear distortion also reduced by same factor as the gain.

Input resistance

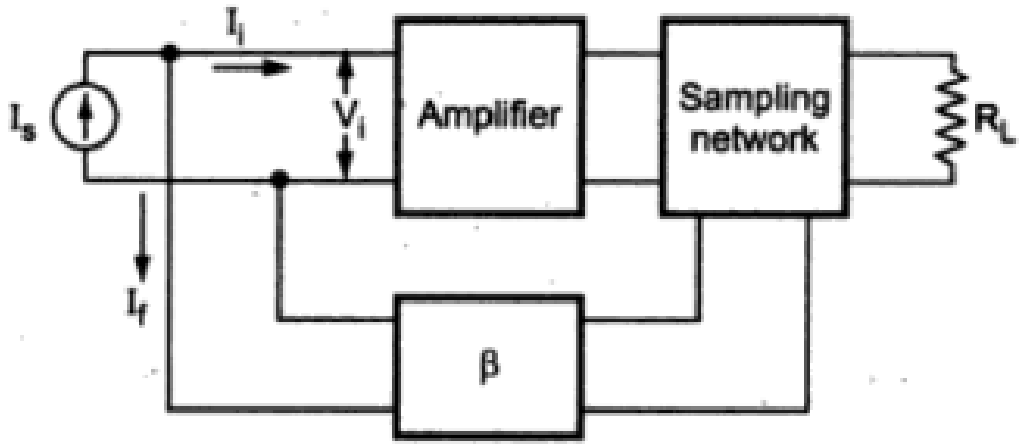
Input resistance

▶ Figure 7.11



If the feedback signal is added to the input in series with the applied voltage (regardless of whether the feedback is obtained by sampling the output current or voltage), it increases the input resistance. Since the feedback voltage V_f opposes V_s, the input current I_i is less than it would be if V_f were absent, as shown in the Fig. 7.11.

▶ **Figure 7.12**



Hence, the input resistance with feedback $R_{if} = \frac{V_s}{I_i}$ is greater than the input resistance without feedback, for the circuit shown in Fig. 7.11.

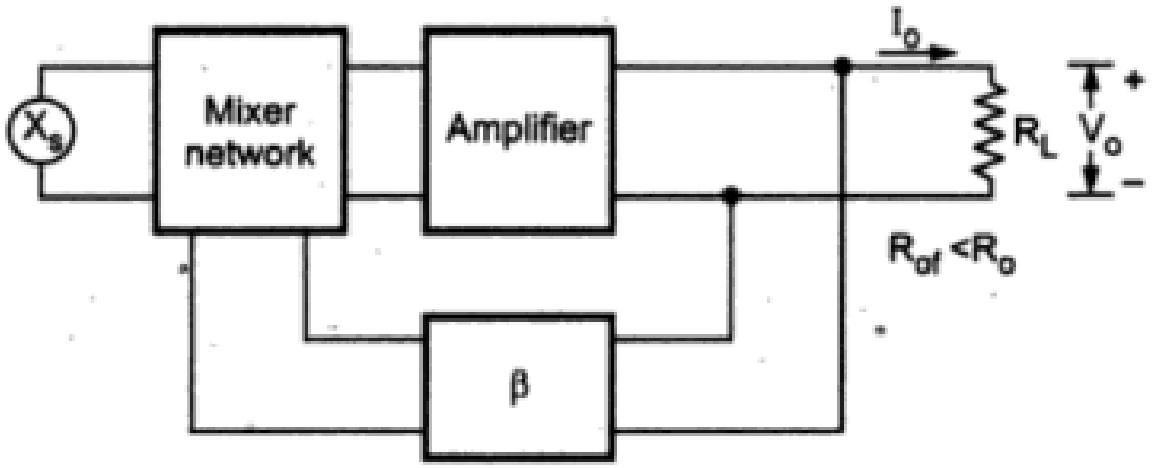
On the otherhand, if the feedback signal is added to the input in shunt with the applied voltage (regardless of whether the feedback is obtained by sampling the output voltage or current), it decreases the input resistance. Since $I_s = I_i + I_f$, the current I_s drawn from the signal source is increased over what it would be if there were no feedback current. as shown in the Fig. 7.12.

Hence, the input resistance with feedback $R_{if} = \frac{V_i}{I_s}$ is decreased for the circuit shown in Fig. 7.12. Now we see the effect of negative feedback on input resistance in different topologies (ways) of introducing negative feedback and obtain R_{if} quantitatively.

Output Resistance

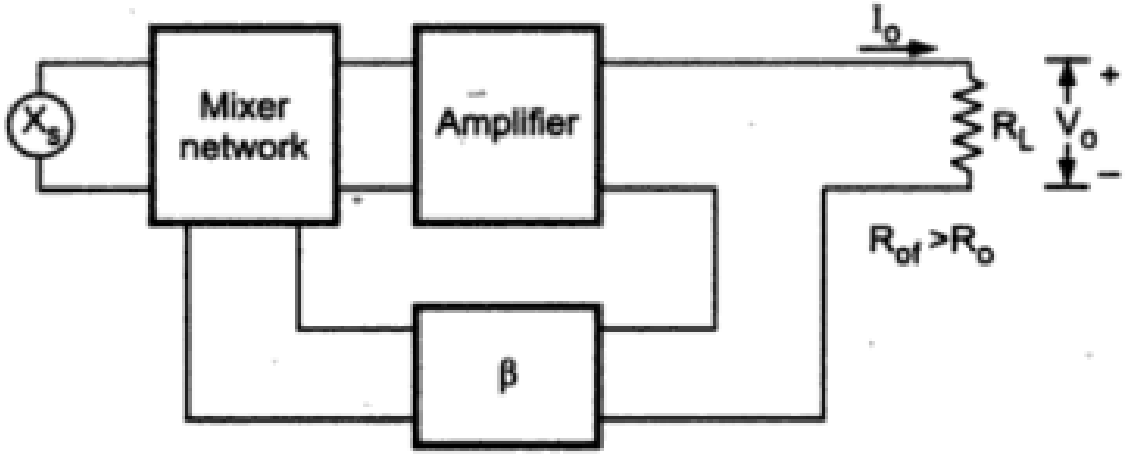
The negative feedback which samples the output voltage, regardless of how this output signal is returned to the input, tends to decrease the output resistance, as shown in the Fig. 7.17.

▶ **Figure 7.17**



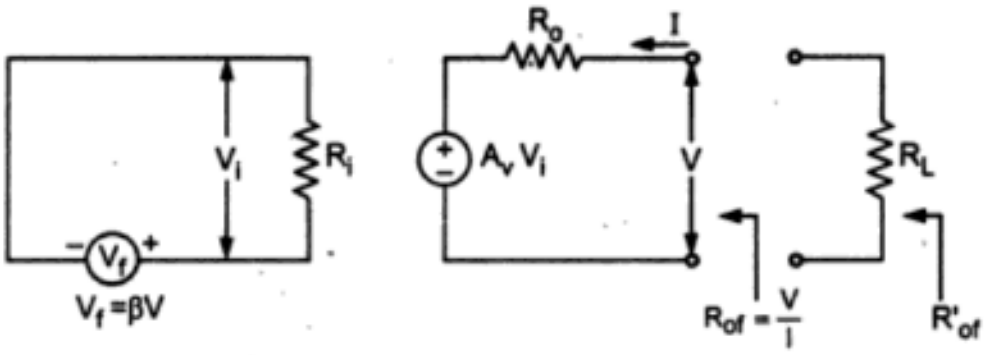
On the other hand, the negative feedback which samples the output current, regardless of how this output signal is returned to the input, tends to increase the output resistance, as shown in the Fig. 7.18.

▶ **Figure 7.18**

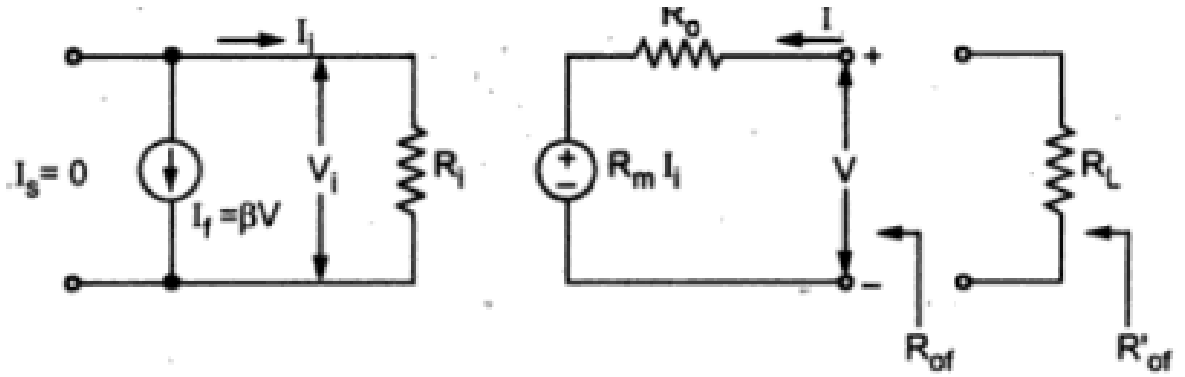


TYPES OF FEED BACK NETWORKS

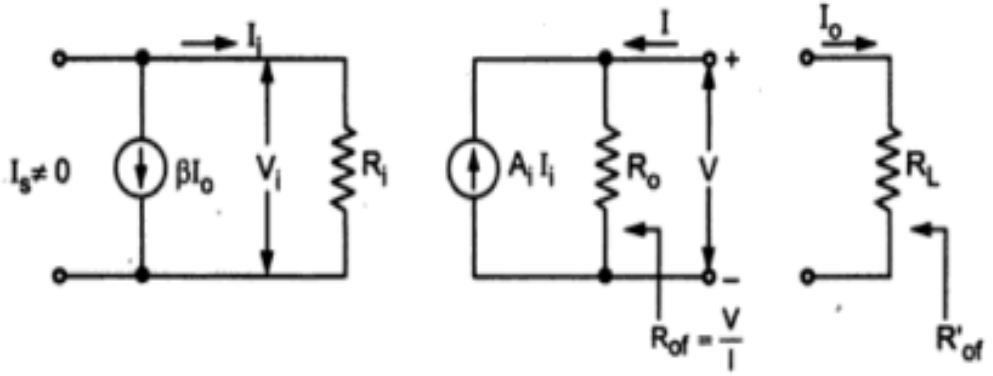
Voltage series feedback



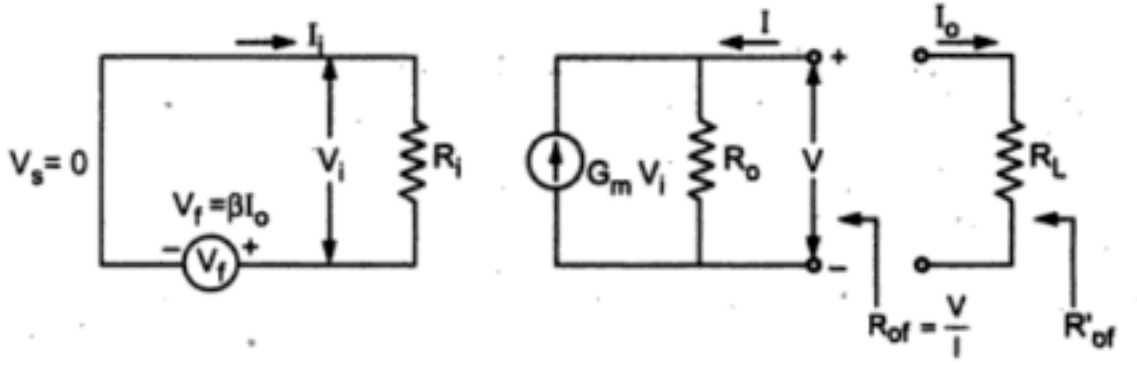
Voltage shunt feedback



Current shunt feedback



Current series feedback



Comparison

Parameter	Voltage series	Current series	Current shunt	Voltage shunt
Gain with feedback	$A_{vf} = \frac{A_v}{1+\beta A_v}$ decreases	$G_{mf} = \frac{G_m}{1+\beta G_m}$ decreases	$A_{if} = \frac{A_i}{1+\beta A_i}$ decreases	$R_{mf} = \frac{R_m}{1+\beta R_{mf}}$ decreases
Stability	Improves	Improves	Improves	Improves
Frequency response	Improves	Improves	Improves	Improves
Frequency distortion	Reduces	Reduces	Reduces	Reduces
Noise and Non linear distortion	Reduces	Reduces	Reduces	Reduces
Input resistance	$R_{if} = R_i(1+\beta A_V)$ increases	$R_{if} = R_i(1+\beta G_M)$ increases	$R_{if} = \frac{R_i}{1+\beta A_I}$ decreases	$R_{if} = \frac{R_i}{1+\beta R_M}$ decreases
Output resistance	$R_{of} = \frac{R_o}{1+\beta A_v}$ decreases	$R_{of} = R_o(1+\beta G_M)$ increases	$R_{of} = R_o(1+\beta A_i)$ increases	$R_{of} = \frac{R_o}{1+\beta R_m}$ decreases

Thank you