UNIT-II

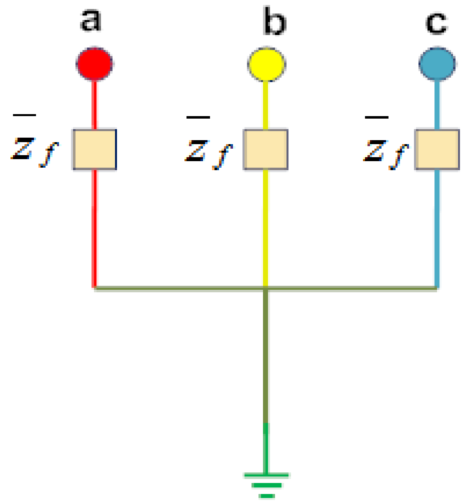
Fault Analysis:

Under normal conditions, a power system operates under balanced conditions with all equipments carrying normal load currents and the bus voltages within the prescribed limits. This condition can be disrupted due to a fault in the system. A fault in a circuit is a failure that interferes with the normal flow of current. A short circuit fault occurs when the insulation of the system fails resulting in low impedance path either between phases or phase(s) to ground. This causes excessively high currents to flow in the circuit, requiring the operation of protective equipments to prevent damage to equipment. The short circuit faults can be classified as:

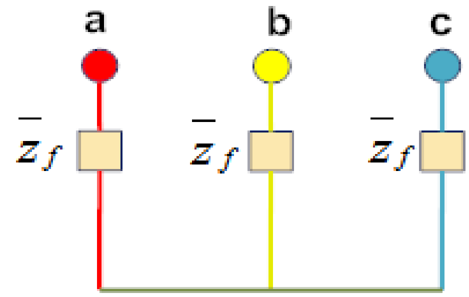
1. Symmetrical faults
2. Unsymmetrical faults

1.Symmetrical faults:

A three phase symmetrical fault is caused by application of three equal fault impedances Z_f to the three phases, as shown in Fig. 4.39. If $Z_f = 0$ the fault is called a solid or a bolted fault. These faults can be of two types: (a) line to line to line to ground fault (**LLLG** fault) or (b) line to line to line fault (**LLL** fault). Since the three phases are equally affected, the system remains balanced. That is why, this fault is called a symmetrical or a balanced fault and the fault analysis is done on per phase basis. The behaviour of **LLLG** fault and **LLL** fault is identical due to the balanced nature of the fault. This is a very severe fault that can occur in a system and if $Z_f = 0$, this is usually the most severe fault that can occur in a system. Fortunately, such faults occur infrequently and only about 5% of the system faults are three phase faults.



(a) LLLG fault



(b) LLL fault

<u>2.TRANSIENT ON A TRANSMISSION LINE</u>

Let us consider the short circuit transient on a transmission line. Certain simplifying assumptions are made at this stage. Knowledge of short circuit current values is necessary for the following reasons.

1. Fault currents which are several times larger than the normal operating currents produce large electromagnetic forces and torques which may adversely affect the stator end windings. The forces on the end windings depend on both the d.c. and a.c. components of stator currents.

2. The electro dynamic forces on the stator end windings may result in displacement of the coils against one another. This may result in loosening of the support or damage to the insulation of the windings.

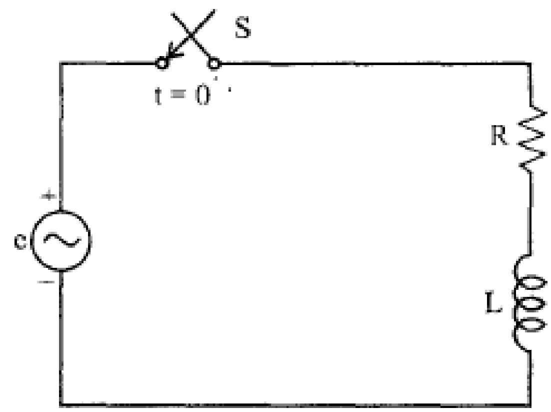
3. Following a short circuit, it is always recommended that the mechanical bracing of the end windings to checked for any possible loosening.

4. The electrical and mechanical forces that develop due to a sudden three phase short circuit are generally severe when the machine is operating under loaded condition.

5. As the fault is cleared with in 3 cycles generally the heating efforts are not considerable.

Short circuits may occur in power systems due to system over voltages caused by lightning or switching surges or due to equipment insulation failure or even due to insulator contamination. Some times even mechanical causes may create short circuits. Other well known reasons include line-to-line, line-to-ground, or line-to-line faults on over head lines. The resultant short circuit has to the interrupted within few cycles by the circuit breaker. It is absolutely necessary to select a circuit breaker that is capable of operating successfully when maximum fault current flows at the circuit voltage that prevails at that instant. An insight can be gained when we consider an R-L circuit connected to an alternating voltage source, the circuit being switched on through a switch.

Consider the circuit in the Fig.



Let $e = E_{max} \text{Sin}(\omega t + \alpha)$ when the switch S is closed at $t = 0^+$

$$e = E_{max} \text{Sin}(\omega t + \alpha) = R + L\frac{di}{dt}$$

α is determined by the magnitude of voltage when the circuit is closed.

The general solution is

$$i = \frac{E_{max}}{|Z|}\left[\text{Sin}\ (\omega t + \alpha - \theta) - e^{\frac{-Rt}{L}}\ \text{Sin}\ (\alpha - \theta)\right]$$

where $|Z| = \sqrt{R^2 + \omega^2 L^2}$

and $\theta = \text{Tan}^{-1}\ \frac{\omega L}{R}$

The current contains two components :

$$\text{a.c. component} = \frac{E_{max}}{|Z|}\ \text{Sin}\ (\omega t + \alpha - \theta)$$

and $$\text{d.c. component} = \frac{E_{max}}{|Z|}\ e^{\frac{-Rt}{L}}\ \text{Sin}\ (\alpha - \theta)$$

If the switch is closed when $\alpha - \theta = \pi$ or when $\alpha - \theta = 0$

the d.c. component vanishes.

the d.c. component is a maximum when $\alpha - \theta = \pm\ \frac{\pi}{2}$

3. Three Phase Short Circuit on Unloaded Synchronous Generator

If a three phase short circuit occurs at the terminals of a salient pole synchronous we obtain typical oscillograms as shown in Fig. 1.2 for the short circuit currents the three phases.

Fig. 1.3 shows the alternating component of the short circuit current when the d.c. component is eliminated. The fast changing sub-transient component and the slowly changing transient Components are shown at A and C. Figure 1.3 shows the electrical torque. The changing field Current is shown in Fig. 1.4

From the oscillogram of a.c. component the quantities x''_d, x''_q, x'_d and x'_q can be determined.

If V is the line to neutral prefault voltage then the a.c. component.

$i_{ac} = \frac{V}{x''_q} = I''$, the r.m.s subtransient short circuit. Its duration is determined by T''_d, the subtransient direct axis time constant. The value of i_{ac} decreases to $\frac{V}{x'_d}$ when $t > T''_d$

with T'_d as the direct axis transient time constant when $t > T'_d$

$$i_{ac} = \frac{V}{x_d}$$

The maximum d.c. off-set component that occurs in any phase at $\alpha = 0$ is

$$i_{d.c,\ max}(t) = \sqrt{2}\frac{V}{x''_d}e^{-t/T_A}$$

where T_A is the armature time constant.

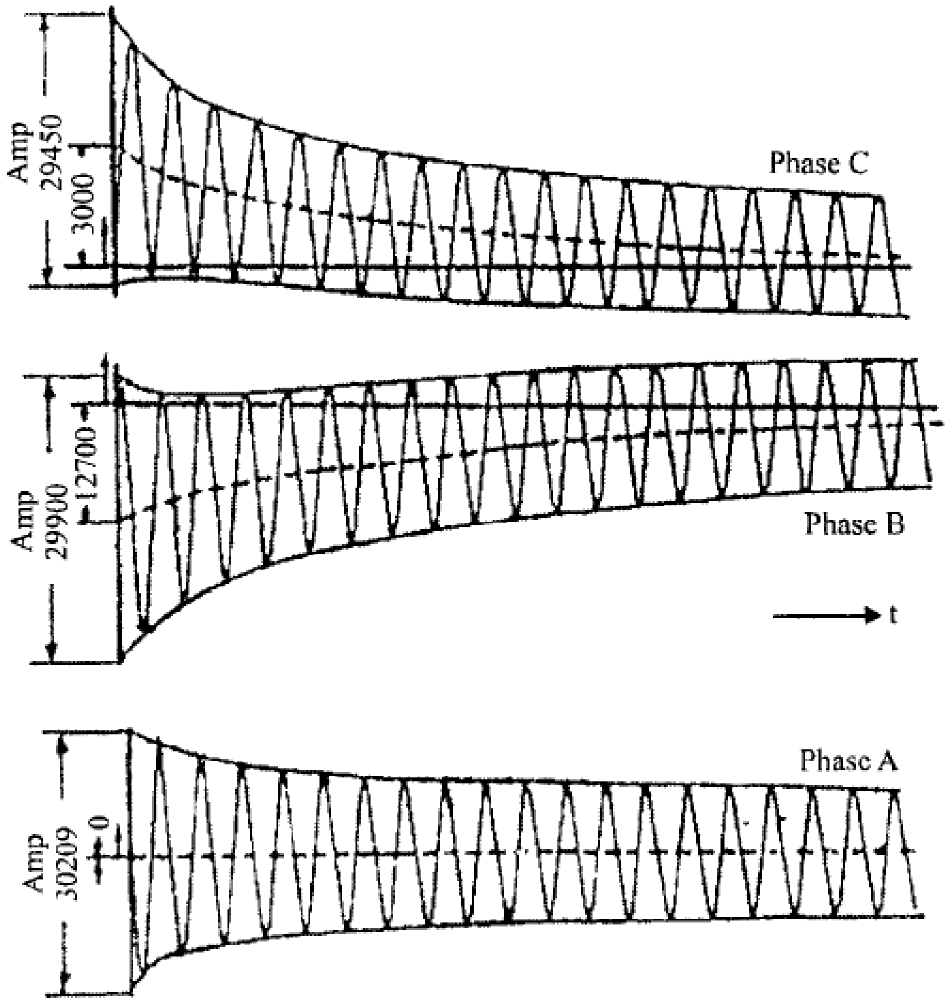


Fig. 1.2 Oscillograms of the armature currents after a short circuit

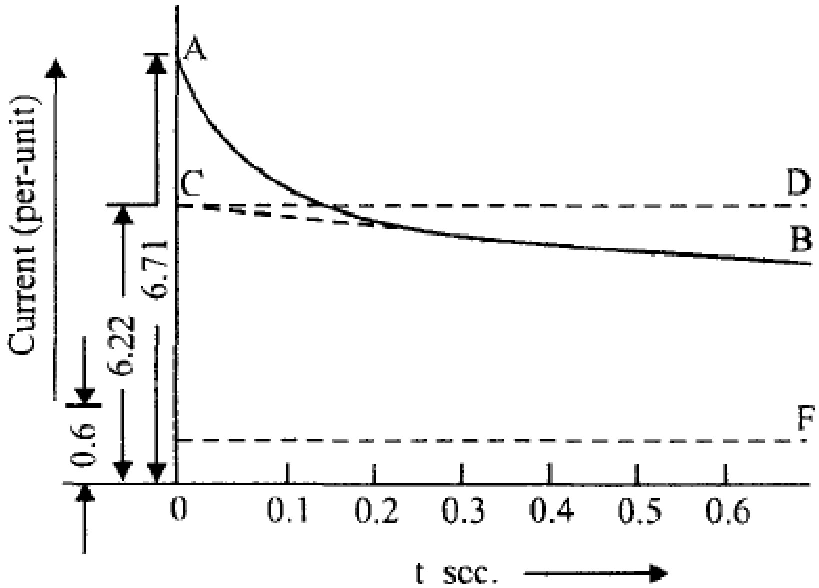


Fig. 1.3 a Alternating component of the short circuit armature current

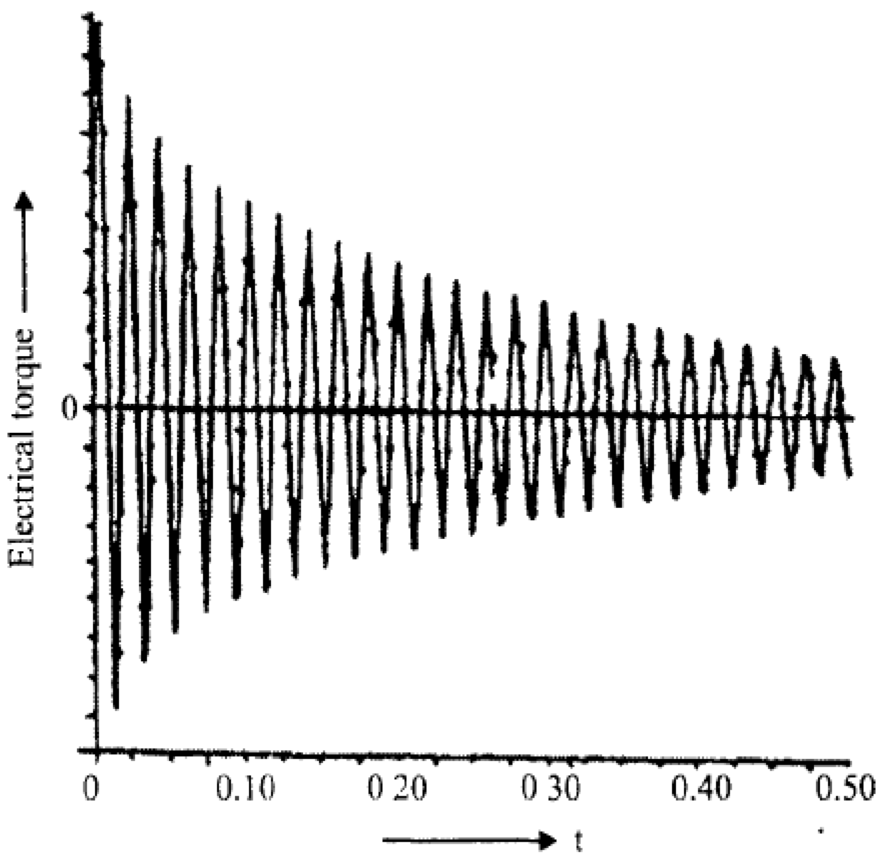


Fig. 1.3 b Electrical torque on three-phase termlnaJ short circuit.

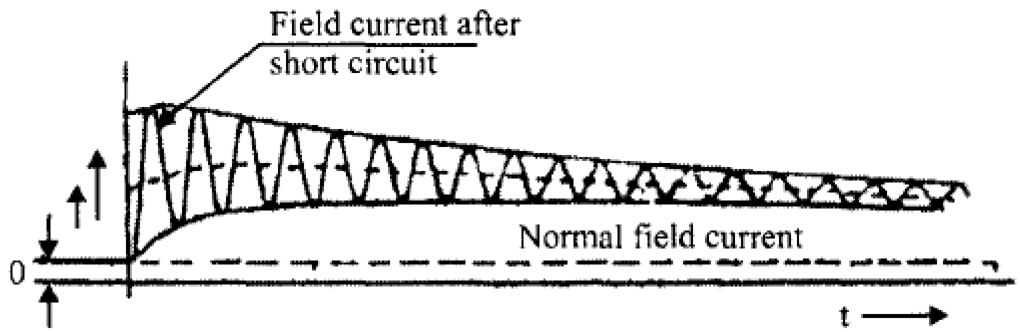


Fig. 1.3 c Oscilogram of the field current after a short circuit.

4. Short Circuit in an Unloaded Synchronous Generator

Fig. 4.1 shows a typical response of the armature current when a three-phase symmetrical short circuit occurs at the terminals of an unloaded synchronous generator.

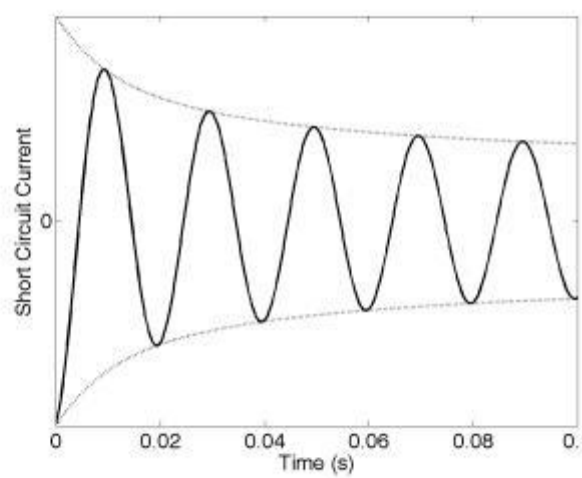


Fig. 4.1 Armature current of a synchronous generator as a short circuit occurs at its terminals.

It is assumed that there is no dc offset in the armature current. The magnitude of the current decreases exponentially from a high initial value. The instantaneous expression for the fault current is given by

$$i_f(t) = \sqrt{2}V_t\left[\left(\frac{1}{X_d''} - \frac{1}{X_d'}\right)e^{-t/T_d''} + \left(\frac{1}{X_d'} - \frac{1}{X_d}\right)e^{-t/T_d'} + \frac{1}{X_d}\right]\sin(\omega t + \alpha - \pi/2)$$ -----------(1)

where V_t is the magnitude of the terminal voltage, α is its phase angle and

X_d'' is the direct axis subtransient reactance

X_d' is the direct axis transient reactance

X_d is the direct axis synchronous reactance

with $X_d'' < X_d' < X_d$. The time constants are

T_d'' is the direct axis subtransient time constant

T_d' is the direct axis transient time constant

In the expression of (1) we have neglected the effect of the armature resistance hence α = π/2. Let us

$$I_f(0) = I_f'' = \frac{V_t}{X_d''} \qquad (2)$$

assume that the fault occurs at time t = 0. From (1) we get the rms value of the current as

which is called the **subtransient fault current**. The duration of the subtransient current is dictated by the time constant T_d''. As the time progresses and $T_d'' < t < T_d'$, the first exponential term of (1) will start decaying and will eventually vanish. However since t is still nearly equal to zero, we have the following

$$I_f' = \frac{V_t}{X_d'} \qquad (3)$$

rms value of the current

This is called the **transient fault current**. Now as the time progress further and the second exponential

$$I_f = \frac{V_t}{X_d} \qquad (4)$$

term also decays, we get the following rms value of the current for the sinusoidal steady state

In addition to the ac, the fault currents will also contain the dc offset. Note that a symmetrical fault occurs when three different phases are in three different locations in the ac cycle. Therefore the dc offsets in the three phases are different. The maximum value of the dc offset is given by

$$i_{dc}^{max} = \sqrt{2} I_f'' e^{-t/T_A} \quad (5)$$

where T_A is the armature time constant.

Consider a single phase alternator operating under no load condition. This alternator is suddenly short circuited. As discussed earlier during initial moment of short circuit only leakage reactance of the machine limits the short circuit current. Under steady state, the armature reaction produces a demagnetizing flux which we take as synchronous reactance. Let the resistance of armature winding be small and can be neglected.

Immediately after the short circuit, the D.C. offset currents appear in the armature winding which can be computed separately on an empirical basis. Thus symmetrical short circuit currents are to considered only. Due to theorem of constant flux linkages, the air gap flux cannot change instantaneously for counterbalancing the demagnetizing effect of armature circuit current, the current is initially limited by leakage reactance only. The currents are thus induced in the field winding and the damper winding in a direction to help the main flux. Thus reactances X_f, X_d are in parallel with X_a during initial period. The equivalent circuit is shown in the Fig. 1. and the equivalent reactance in this case is called subtransient reactance.

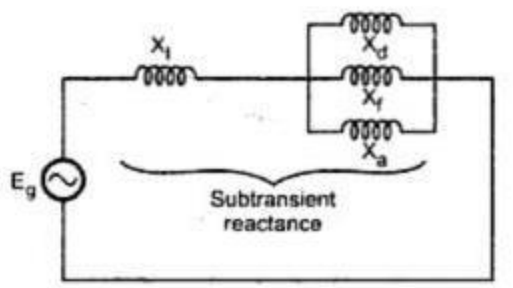


Fig. 1

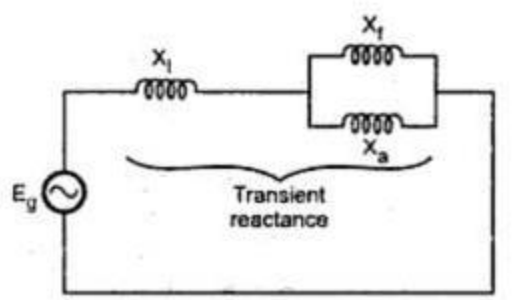


Fig. 2

These currents appearing in the damper winding and the field winding decay depending upon winding time constants The damper winding has inductance less than that of field winding and hence current in it dies out first and afterwords X_d is said to be effectively open circuited. The machine reactance changes from its value of subtransient to transient consisting of parallel combination of X_f and X_{ad}. This is shown in the Fig. 2.

The current in the field winding also dies out and we say that the machine is operating in the combination of X_f and X_a. The equivalent circuit at steady state is shown in the Fig. 3.

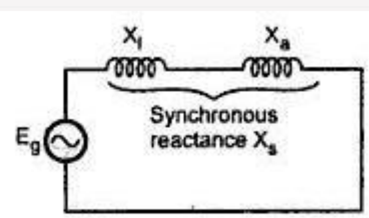


Fig. 3

The subtransient and transient reactances are respectively given by,

$$\text{Subtransient reactance,} \quad X''_d = X_l + \frac{1}{\left(\frac{1}{X_a}\right)+\left(\frac{1}{X_d}\right)+\left(\frac{1}{X_f}\right)}$$

$$\text{Transient reactance,} \quad X'_d = X_l + \frac{1}{\left(\frac{1}{X_a}\right)+\left(\frac{1}{X_f}\right)}$$

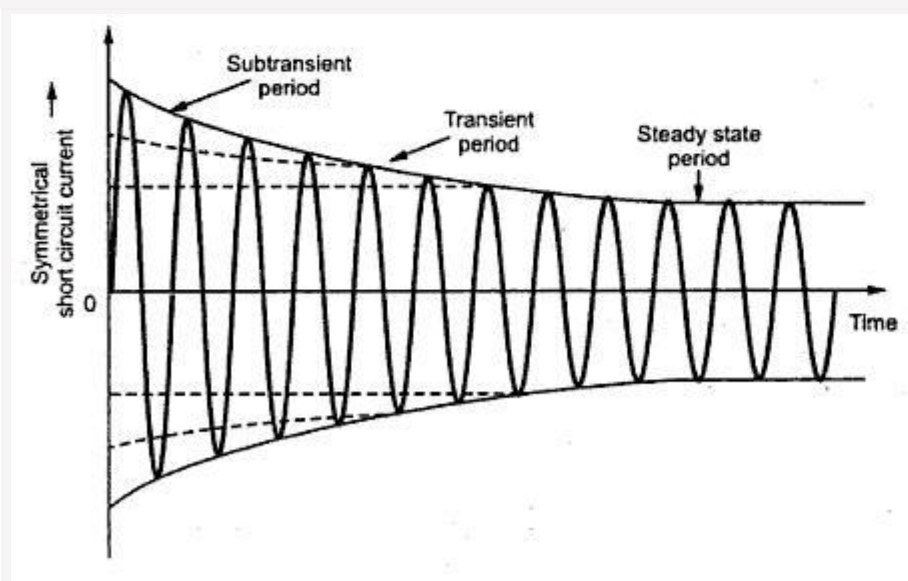
It can be seen that X'' X' X. Thus the machine offers variable reactance. As X'' is smallest initially current is very large which is reduced subsequently when currents in damper winding and field winding die out.

The currents are given by,

$$I'' = \frac{E_g}{X''_d}$$

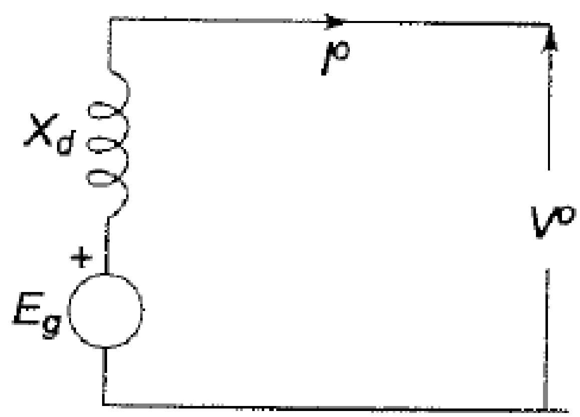
$$I' = \frac{E_g}{X'_d}$$

The oscillogram of current neglecting d.c. offset currents is shown in the Fig. 4.



5. Short circuit of a loaded synchronous machine

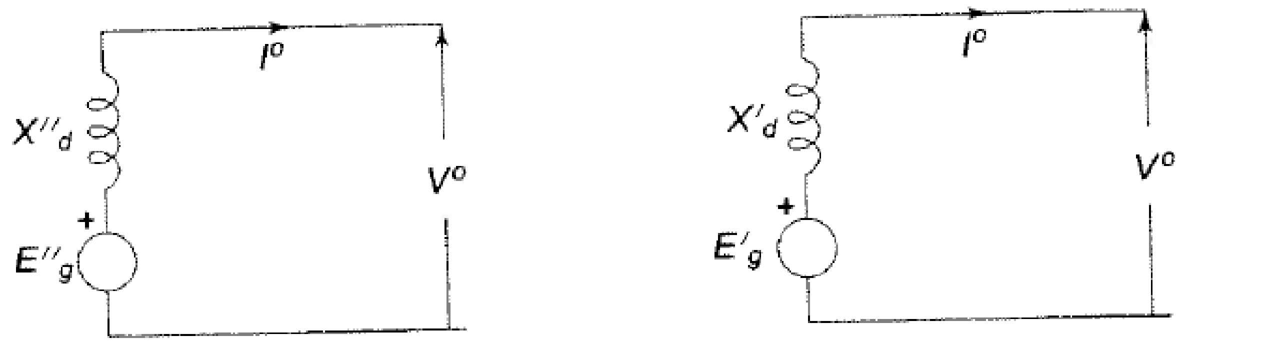
Figure 5.1 shows the circuit model of a synchronous generator operating under steady conditions supplying a load current I^o to the bus at a terminal voltage of V^0 .E_g is the induced emf under loaded condition and Xd is the direct axis synchronous reactance of the machine. When short circuit occurs at the terminals of this machine, the circuit model to be used for computing short circuit current is given in Fig.5.2 a for subtransient current, and in Fig. 5.2b for transient current. The induced emfs to be used in these models are given by



5.1 Circuit model of a loaded machine

$$E_g'' = V^o + jI^oX_d''$$
$$E_g' = V^o + jI^oX_d'$$

The voltage E_g"is known as the voltage behind the subiransient reactance and the voltage E'$_g$is known as the voltage behind the transient reactance. In fact, if 1° is zero (no load case), Eg"= Eg' = Eg the no load voltage.



(a) Circuit model for computing subtransient current

(b) Circuit model for computing transient current

Synchronous motors have internal emfs and reactances similar to that of a generator except that the current direction is reversed. During short circuit conditions these can be replaced by similar circuit models except that the vo1tae behind subtransient /transient reactance is given by

$$E''_m = V^o - jI^oX''_d$$
$$E'_m = V^o - jI^oX'_d$$

Whenever we are dealing with short circuit of an interconnected system, the synchronous machines (generators and motors) are replaced by their corresponding circuit models having voltage behind subtransient (transient) reactance in series with subtransient (transient) reactance. The rest of the network being passive remains unchanged.

6. Short Circuit (SC) Current Computation through the Thevenin Theorem

An alternate method of computing short circuit currents is through the application of the Thevenin theorem. This method is faster and easily adopted to systematic computation for large networks. While the method is perfectly general1 it is illustrated here through a simple example. Consider a synchronous generator feeding a synchronous motor over a line. Figure 6.1 a shows the circuit model of the system under conditions of steady load. Fault computations are to be made for a fault at *F*, at the motor terminals. As a first step the circuit model is replaced by the one shown in Fig.6.1d, wherein the synchronous machines are represented by their transient reactances (or subtransient reactances if subtransient currents are of interest) in series with voltages behind transient reactances. This change does not disturb the prefault current I º and prefault voltage *V*° (at *F)*.

As seen from *FG* the Thevenin equivalent circuit of Fig.6.1a ,b is drawn in Fig. 6.2c. it comprises prefault voltage *V*° in series with the passive Thevenin impedance network. it is noticed that the prefault current I^o does not appear in the passive Thevenin impedance network. It is therefore to the remembered that this current must be accounted for by superposition after the SC solution is obtained through use of the Thevenin equivalent. Consider now a fault at *F* through an impedance *Z'*. Figure 6.1 d shows the Thevenin equivalent of the system feeding the fault impedance. We can immediately write

$$I^f = \frac{V^o}{jX_{Th} + Z^t}$$

Current caused by fault in generator circuit

$$\Delta I_g = \frac{X'_{dm}}{(X'_{dg} + X + X'_{dm}} I^f$$

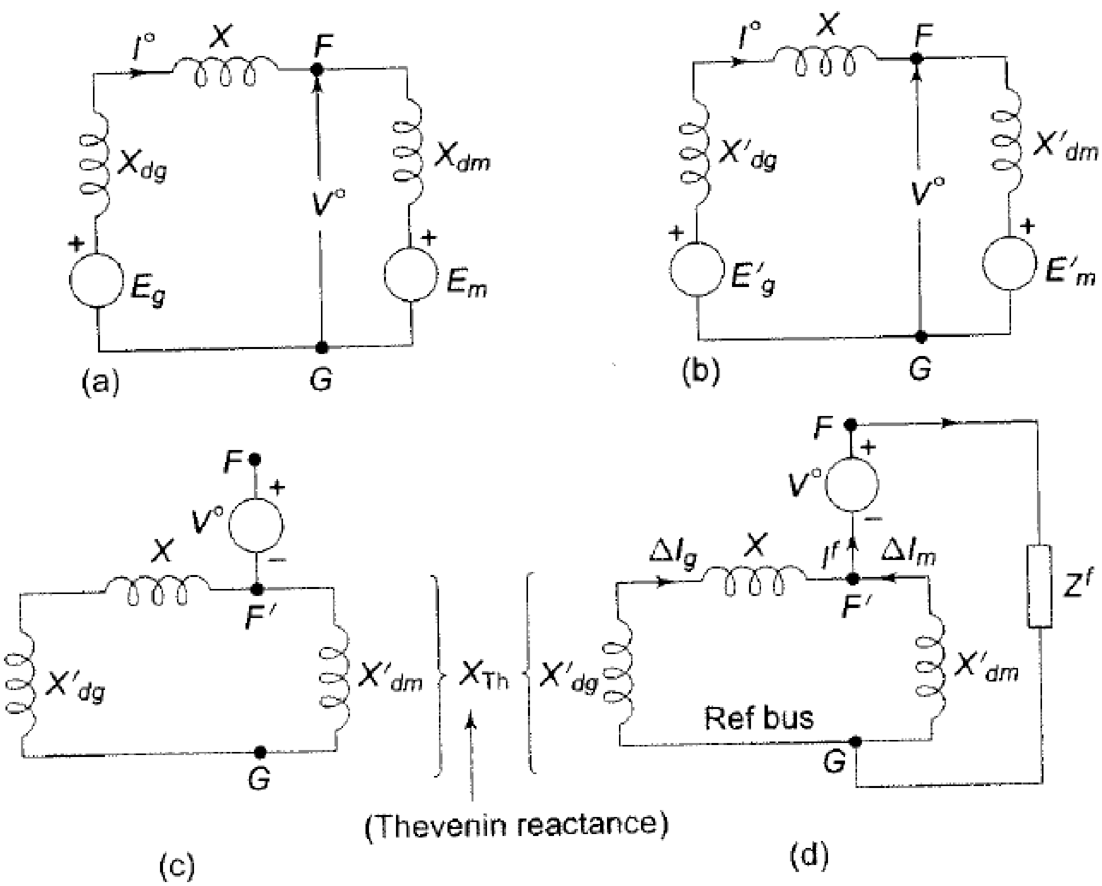


Fig. 6.2 Computation ot SC current by the Thevenin equivalent

Current caused by fault in motor circuit

$$\Delta I_m = \frac{X'_{dg} + X}{(X'_{dm} + X + X'_{dg})} I^f$$

Postfault currents and voltages are obtained as follows by superposition:

$I_g^f = I^o + \Delta I_g$

$I_m^f = -I^o + \Delta I_m$ (in the direction of ΔI_m) (

Postfault voltage

$$V^f = V^o + (-jX_{Th}I^f) = V^o + \Delta V$$

An observation can be made here. Since the prefault current flowing out of fault point *F* is always zero, the postfault current out of *F* is independent of load for a given prefault voltage at *F*.

The above approach to SC computation is summarized in the following four steps:
Step 1: Obtain steady state solution of loaded system (load flow study).

Step 2: Replace reactances of synchronous machines by their subtransient/ transient values. Short circuit all emf sources. The result is the passive Thevenin network.

Step 3. Excite the passive network of Step 2 at the fault point by negative of prefault voltage (see Fig. 6.2 d) in series with the fault impedance. Compute voltages and currents at all points of interest.

Step 4: Postfaujt currents and voltages are obtained by adding results of Steps 1 and3.

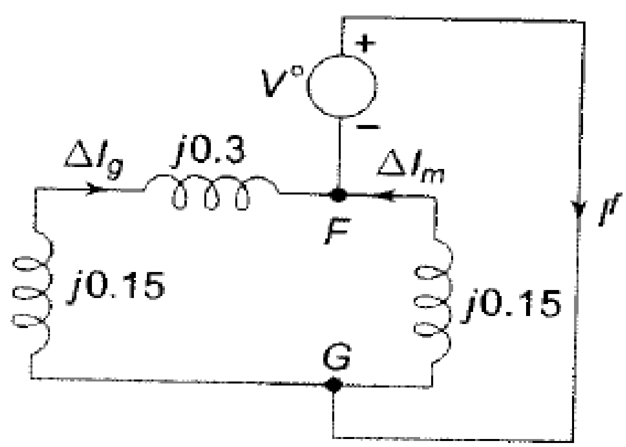


Fig. 6.3 *F* is the fault point on the passive Thevenin network

7. SELECTION OF CIRCUIT BREAKERS

Two of the circuit breaker ratings which require the computation of SC current are: *rated momentary current* and *rated symmetrical interrupting current.* Symmetrical SC current is obtained by using subtransient reactances for synchronous machines. Momentary current (rms) is then calculated by multiplying the symmetrical momentary current by a factor of 1.6 to account for the presence of DC off-set current.

Symmetrical current to be interrupted is computed by using subtransient reactances for synchronous generators and transient reactances for synchronouS motors—induction motors are neglected*. The DC off-set value to be added to obtain the current to be interrupted is accounted for by multiplying the symmetrical SC current by a factor as tabulated below:

Circuit Breaker Speed Multiplying Factor

8 cycles or slower	1
5 cycles	1.1
3 cycles	1.2
2 cycles	1.3

If SC MVA (explained below) is more than 500, the above multiplying factors are increased by 0.1 each. The multiplying factor for air breakers rated 600 V or lower is 1.25. The current that a circuit breaker can interrupt is inversely proportional to the operating voltage over a certain range, i.e.

Amperes at operating voltage

= amperes at rated voltage x rated voltage/operating voltage

Of course, operating voltage cannot exceed the maximum design value. Also, no matter how low the voltage is, the rated interrupting current cannot exceed the *rated maximum interrupting current*. Over this range of voltages, the product of operating voltage and interrupting current is constant. It is therefore logical as well as convenient to express the circuit breaker rating in terms of SC MVA that can be interrupted, defined as

Rated interrupting MVA (three-phase) capacity $= \sqrt{3}|V(line)|rate|I(line)|\text{int}\ errupted\ crrent$

where V(Iine) is in kV and *1* (line) is kA.
Thus, instead of computing the SC current to be interrupted, we compute three-phase SC MVA to be interrupted, where
SC MVA (3-phase) = $\sqrt{3}$ x prefault line voltage in kV x SC current in kA.

8. ALGORITHM FOR SHORT CIRCUIT STUDIES

So far we have carried out short circuit calculations for simple systems whose passive networks can be easily reduced. In this section we extend our study to large systems. In order to apply the four steps of short circuit computation developed earlier to large systems it is necessary to evolve a systematic general algorithm so that a digital computer can be used.

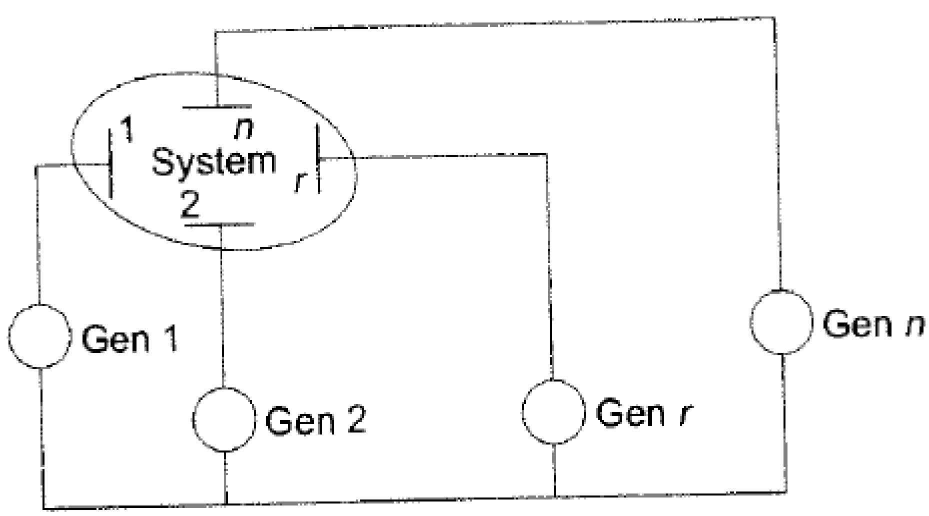


Fig. 8.1 n-bus system under steady load

Consider an n-bus system shown schematically in Fig.8.1 operating at steady load. The first step towards short circuit computation is to obtain prefault voltages at all buses and currents in all lines through a load flow study. Let us indicate the prefault bus voltage vector as

$$V_{\mathrm{BUS}}^{0} = \begin{bmatrix} V_1^0 \\ V_2^0 \\ \vdots \\ V_n^0 \end{bmatrix}$$

Let us assume that the rth bus is faulted through a fault impedance Z^f. The postfault bus voltage vector will be given by

$$\boldsymbol{V}_{\mathrm{BUS}}^{f} = \boldsymbol{V}_{\mathrm{BUS}}^{0} + \Delta \boldsymbol{V}$$

where ΔV is the vector of changes in bus voltages caused by the fault.

As step 2, we drawn the passive Thevenin network of the system with generators replaced by transient / sub transient reactance's with their emfs shorted (Fig.8.2).

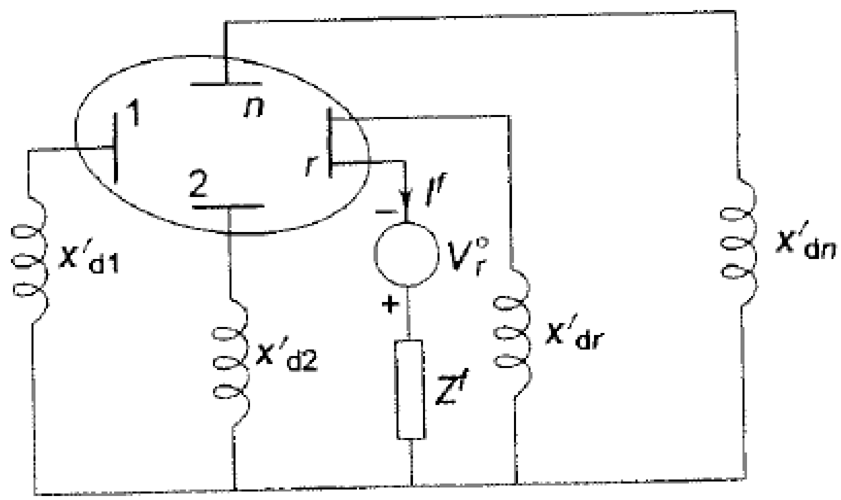


Fig. 8.2 Network of the system of Fig. *8.1* for computing changes in bus voltages caused by the fault

As per step 3 we now excite the passive Thevenin network with — V_r^o in series with Z^f as in Fig. 8.2 The vector ΔV comprises the bus voltages of this network.
Now

$$\Delta \boldsymbol{V} = \boldsymbol{Z}_{\text{BUS}} \boldsymbol{J}^f$$

where

$$Z_{BUS} = \begin{bmatrix} Z_{11} & \dots & Z_{1n} \\ \vdots & & \vdots \\ Z_{n1} & \dots & Z_{nn} \end{bmatrix}$$ = bus impedance matrix of the passive Thevenin network

J^f = bus current injection vector

Since the network is injected with current $-I^f$ only at the rth bus,

$$J^f = \begin{bmatrix} 0 \\ 0 \\ \vdots \\ I_r^f = -I^f \\ \vdots \\ 0 \end{bmatrix}$$

$$\Delta V_r = -Z_{rr} I^f$$

By step 4, the voltage at the rth bus under fault is

$$V_r^f = V^0{}_r + \Delta V^0{}_r = V^0{}_r - Z_{rr} I^f$$

However, this voltage must equal

$$V_r^f = Z^f I^f$$

$$Z^f I^f = V_r^0 - Z_{rr} I^f$$

$$I^f = \frac{V_r^0}{Z_{rr} + Z^f}$$

$$V_r^f = \frac{Z^f}{Z_{rr} + Z^f} V_r^0$$

9. Zbus formation

By Inventing Y_{BUS}

$$J_{BUS} = Y_{BUS}\ V_{BUS}$$

or $$V_{BUS} = [Y_{BUS}]^{-1}\ J_{BUS} = Z_{BUS}\ J_{BUS}$$

or $$Z_{BUS} = [Y_{BUS}]^{-1}$$

The sparsity of BUS may be retained by using an efficient inversion technique and nodal impedance matrix can then be calculated directly from the factorized admittance matrix.

Current Injection Technique

we can be written in the expanded **form**

V1=Z11 I1+Z12 I2+………..+Z1N In
V2=Z21 I1+Z22 I2+………..+Z2N In
.
.
.
Vn=Zn1 I1+Zn2 I2+………..+Znn In

It immediately follows

$$Z_{ij} = \frac{V_i}{I_j}\ for\ I_1 = I_2 .... = I_n = 0\ and\ I_j \neq 0$$

Zbus build algorithm

It is a step-by-step programmable technique which proceeds branch by branch. It has the advantage that any modification of the network does not require complete rebuilding of ZBUS Consider that ZBUS has been formulated upto a certain stage and another branch is now added. Then

Z b branch impedance

ZBUS (old)+Zb=Znew bus

Upon adding a new branch, one of the following situations is presented.

1. Zb is added from a new bus to the reference bus (i.e. a new branch is added and the dimension of ZBUS goes up by one). This is type-1 modification

2. Zb is added from a new bus to an old bus (i.e., a new branch is added and the dimension of ZBus goes up by one). This is rype-2 modification.

3. Zb connects an old bus to the reference branch (i.e., a new loop is formed but the dimension of Zbus does not change). This is type-3 modification.

4. Zb connects two old buses (i.e., new loop is formed but the dimension of ZBIs does not change). This is type-4 modification.

5. Zb connects two new buses (ZBUS remains unaffected in this case). This situation can be avoided by suitable numbering of buses and from now onwards will be ignored. Notation: i, j—old buses; r—reference bus; k—new bus.

Type-I Modification

Figure 9.1shows a passive (linear) n-bus network in which branch with impedance *Zb* is added to the new bus *k* and the reference bus *r*. **Now**

$$V_k = Z_b I_k$$

$$Z_{ki} = Z_{ik} = 0;\ i = 1, 2, \ldots, n$$

$$\therefore \qquad Z_{kk} = Z_b$$

Hence

$$Z_{BUS}\ (\text{new}) = \left[\begin{array}{ccc|c} & & & 0 \\ & Z_{Bus}(\text{old}) & & \vdots \\ & & & 0 \\ \hline 0 & & \ldots 0 & Z_b \end{array}\right]$$

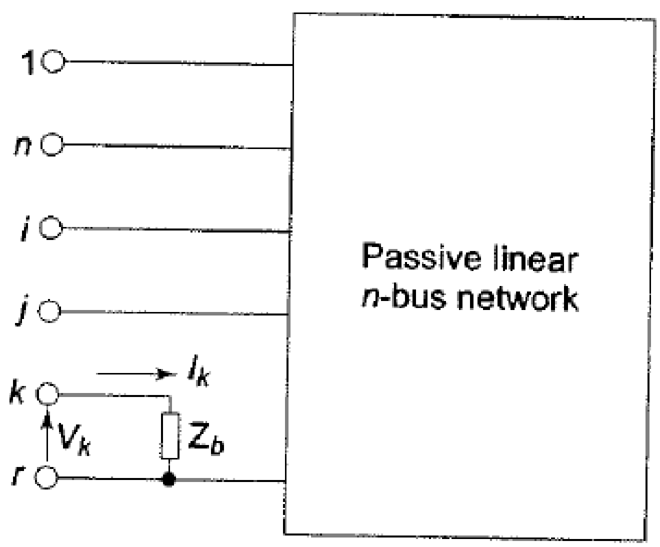


Fig. 9.1 Type-I modification

Type-2 Modification

Zb is added from new bus *k* to the old bus j as in Fig. 9.2. It follows from this figure that

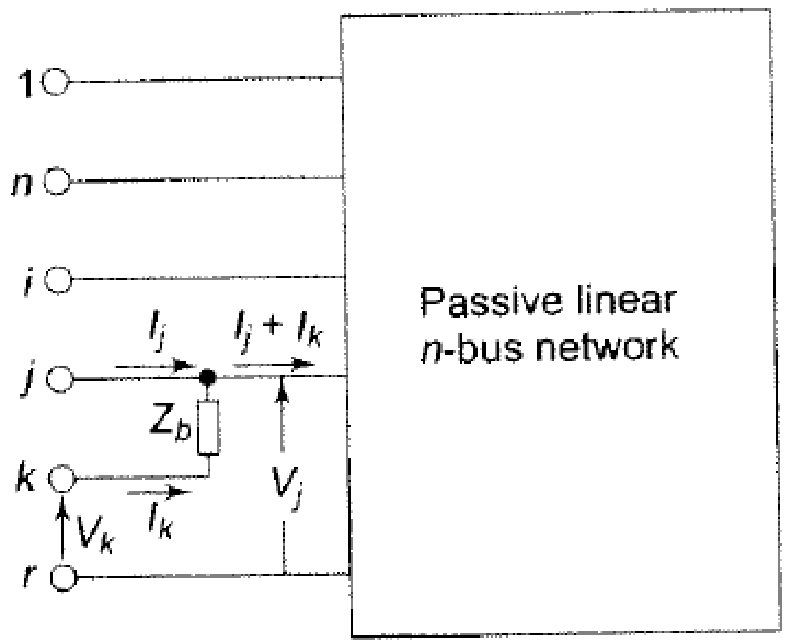


Fig. 9.2 Type-2 modification

$$V_k = Z_b I_k + V_j$$
$$= Z_b I_k + Z_{j1} I_1 + Z_{j2} I_2 + \ldots + Z_{jj}\ (I_j + I_k) + \ldots + Z_{jn} I_n$$

Rearranging,

$$V_k = Z_{j1} I_1 + Z_{j2} I_2 + \ldots + Z_{jj} I_j + \ldots + Z_{jn} I_n + (Z_{jj} + Z_b) I_k$$

Consequently

$$Z_{BUS}\ (\text{new}) = \left[\begin{array}{c|c} & Z_{1j} \\ & Z_2 j \\ Z_{BUS}(\text{old}) & \vdots \\ & Z_{nj} \\ \hline Z_{ji} Z_{j2} \ldots Z_{jn} & Z_{jj} + Z_b \end{array}\right]$$

Type 3 modification

Zb connects an old bus (j) to the reference bus *(r)* as in Fig. 9.3 This case follows from Fig. *9.25* by connecting bus *k* to the reference bus *r*, i.e. by setting *Vk*= 0.

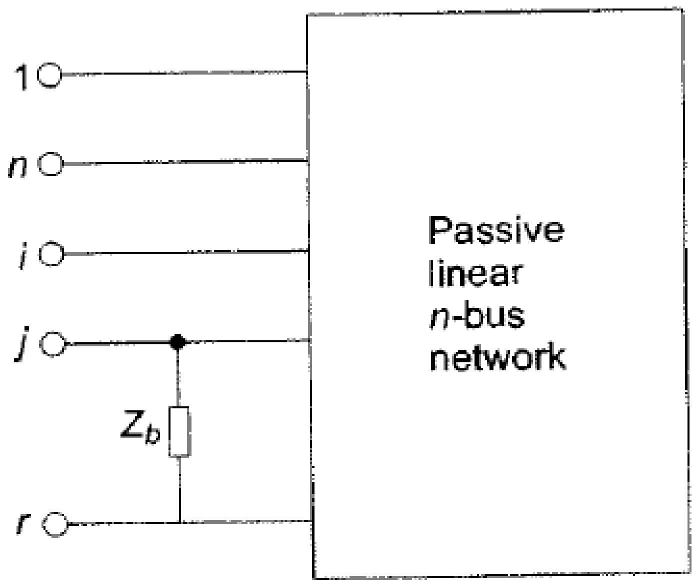


Fig. 9.3 Type-3 modification

Thus

$$\begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_n \\ 0 \end{bmatrix} = \left[\begin{array}{c|c} & Z_{1j} \\ & Z_2 j \\ Z_{\text{BUS}}(\text{old}) & \vdots \\ & Z_{nj} \\ \hline Z_{j1} Z_{j2} \ldots Z_{jn} & Z_{jj} + Z_b \end{array}\right] \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_n \\ I_k \end{bmatrix}$$

Eliminate I_k in the set of equations contained in the matrix operation

$$0 = Z_{j1} I_1 + Z_{j2} I_2 + \ldots + Z_{jn} I_n + (Z_{jj} + Z_b) I_k$$

or

$$I_k = -\frac{1}{Z_{jj} - Z_b} (Z_{j1} I_1 + Z_{j2} I_2 + \ldots + Z_{jn} I_n)$$

Now

$$V_i = \left[Z_{i1} - \frac{1}{Z_{jj} + Z_b}(Z_{ij} Z_{j1})\right] I_1 + \left[Z_{i2} - \frac{1}{Z_{jj} + Z_b}(Z_{ij} Z_{j2})\right] I_2$$

$$+ \ldots + \left[Z_{in} - \frac{1}{Z_{jj} + Z_b}(Z_{ij}\ Z_{jn})\right] I_n$$

$$Z_{\text{BUS}}\ (\text{new}) = Z_{\text{BUS}}\ (\text{old} - \frac{1}{Z_{jj} + Z_b} \begin{bmatrix} Z_{1j} \\ \vdots \\ Z_{nj} \end{bmatrix} [Z_{j1} \ldots Z_{jn}]$$

Type-4 modification

Zb connects two old buses as in Fig. 9.4. Equations can be written as follows for all the network buses.

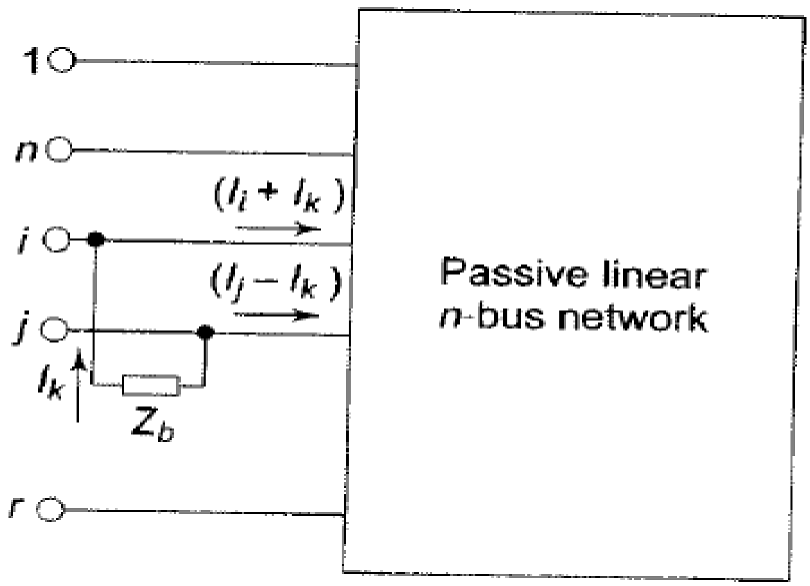


Fig. 9.4 Type-4 modification

$$V_i = Z_{i1}I_1 + Z_{i2}I_2 + \ldots + Z_{1i}\,(I_i + I_k) + Z_{ij}\,(I_j - I_k) + \ldots + Z_{in}I_n$$

Similar equations follow for other buses.

The' voltages of the buses *I* and j are, however, constrained by' the equation

$$V_j = Z_bI_k + V_i$$

$$Z_{j1}I_1 + Z_{j2}I_2 + \ldots + Z_{ji}\,(I_i + I_k) + Z_{jj}\,(I_j - I_k) + \ldots + Z_{jn}I_n$$
$$= Z_bI_k + Z_{i1}I_1 + Z_{i2}I_2 + \ldots + Z_{ii}\,(I_i + I_k) + Z_{ij}(I_j - I_k) + \ldots + Z_{in}I_n$$

$$0 = (Z_{i1} - Z_{j1})\, I_1 + \dots + (Z_{ii} - Z_{ji})\, I_i + (Z_{ij} - Z_{jj})\, I_j + \dots + (Z_{in} - Z_{jn})\, I_n + (Z_b + Z_{ii} + Z_{jj} - Z_{ij} - Z_{ji})\, I_k$$

$$\begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_n \\ - \\ 0 \end{bmatrix} = \left[\begin{array}{c|c} Z_{BUS} & \begin{matrix} (Z_{1i} - Z_{1j}) \\ | \\ (Z_{ni} - Z_{nj}) \end{matrix} \\ \hdashline (Z_{i1} - Z_{j1}) \dots (Z_{in} - Z_{jn}) & Z_b + Z_{ii} + Z_{jj} - 2Z_{ij} \end{array}\right] \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_n \\ \hline I_j \end{bmatrix}$$

$$Z_{BUS}\ (new) = Z_{BUS}\ (old) - \frac{1}{Z_b + Z_{ii} + Z_{jj} - 2Z_{ij}} \begin{bmatrix} Z_{1i} & - & Z_{1j} \\ & \vdots & \\ Z_{ni} & - & Z_{nj} \end{bmatrix}$$

$$[Z_{i1} - Z_{j1}] \dots (Z_{in} - Z_{jn})]$$