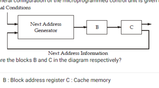
# COA (GATE - 2021) - REPORTS

OVERALL ANALYSIS | COMPARISON REPORT | SOLUTION REPORT

ALL(17) | CORRECT(0) | INCORRECT(0) | SKIPPED(17)

**Q. 1** Solution Video | Have any Doubt ? | Bookmark

The general configuration of the microprogrammed control unit is given below:

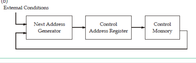



What are the blocks B and C in the diagram respectively?

A. B : Block address register C : Cache memory

B. B : Control address register C : Control memory — Correct Option

**Solution :**
(b)




C. B : Branch register C : Cache memory

D. B : Control address register C : Random access memory

QUESTION ANALYTICS

**Q. 2** Solution Video | Have any Doubt ? | Bookmark

A CPU has 24-bit instructions. A program starts at address 300 (in decimal). Which one of the following is a legal program counter (all values in decimal).

A. 400

B. 500

C. 600 — Correct Option

**Solution :**
(c)
Size of instructions 24 bits.
Starting address of the program is 300. The size of instruction is 3 byte long so that the address is always the multiple of 3 byte, next address is 600, it is also the next instruction of the program.

D. 700

QUESTION ANALYTICS

**Q. 3** Solution Video | Have any Doubt ? | Bookmark

The absolute addressing mode has

A. operand is inside the instruction.

B. address of the operand is inside the instruction — Correct Option

C. register containing the address of the operand is specified inside the instruction.

D. location of the operand is implicit.

QUESTION ANALYTICS

**Q. 4** Solution Video | Have any Doubt ? | Bookmark

The concept of pipelining improves performance by

A. eliminating data hazards

B. decreasing instruction latency

C. decreasing the cache miss rate

D. instruction level parallelism — Correct Option

**Solution :**
(d)
Instruction pipelining is a technique that implements a form of parallelism called instruction level parallelism with a single processor. It therefore allows faster CPU throughput.

QUESTION ANALYTICS

**Q. 5** Solution Video | Have any Doubt ? | Bookmark

Consider the following table:

| Design Change | Effect on miss rate |
|---|---|
| P. Increase cache size | (i) Decrease conflict misses |
| Q. Increase associativity | (ii) Decrease compulsory misses |
| R. Increase block size | (iii) Decrease capacity misses |

Match the Design change in cache to effect on miss rate:

A. P→(i), Q→(ii), R→(iii)

B. P→(i), Q→(iii), R→(ii)

C. P→(ii), Q→(i), R→(iii)

D. P→(iii), Q→(i), R→(ii) — Correct Option

QUESTION ANALYTICS

**Q. 6** Solution Video | Have any Doubt ? | Bookmark

It is required to construct a memory of 1024 words with 4 bytes per word, organized in a matrix having 16 rows and 16 columns, each intersection of row and column stores bit. Then the number of matrices required are _____.

128 — Correct Option

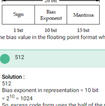
**Solution :**
128

$$\text{Total size of memory} = 1024 \times 4 \times 8 \text{ bits}$$
$$\text{Matrix size} = 16 \times 16 \text{ bits}$$
$$\text{Number of matrices required} = \frac{1024 \times 4 \times 8}{16 \times 16} = 128$$

QUESTION ANALYTICS

**Q. 7** FAQ | Solution Video | Have any Doubt ? | Bookmark

Consider the following hypothetical floating point format.




The bias value in the floating point format when the format uses excess code form is _____.

512 — Correct Option

**Solution :**
512
Bias exponent in representation = 10 bit
$= 2^{10} = 1024$
So, excess code form uses the half of the range as a bias i.e, 512.

QUESTION ANALYTICS

**Q. 8** Solution Video | Have any Doubt ? | Bookmark

Which of the following is a form of memory?

A. Instruction cache — Correct Option

B. Instruction register — Correct Option

C. Instruction opcode

D. Translation look aside buffer — Correct Option

YOUR ANSWER - NA | CORRECT ANSWER - a,b,d | STATUS - SKIPPED

**Solution :**
(a, b, d)
Instruction opcode is not a form of memory.

QUESTION ANALYTICS

**Q. 9** Solution Video | Have any Doubt ? | Bookmark

The performance of a pipelined processor suffers if

A. the pipeline stages have different delays. — Correct Option

B. consecutive instructions are dependent on each other. — Correct Option

C. the pipeline stages share hardware resources. — Correct Option

D. the pipeline stages have same delays.

YOUR ANSWER - NA | CORRECT ANSWER - a,b,c | STATUS - SKIPPED

**Solution :**

QUESTION ANALYTICS

**Q. 10** Solution Video | Have any Doubt ? | Bookmark

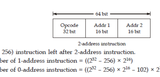
A hypothetical system which has 64 bit instructions and 16 bit address. If there are 102 and 256 1-address and 2-address instructions respectively, then how many 0-address (zero) instructions can be formulated?

A. $((2^{32} - 256 \times 2^{16}) - 102) \times 2^{16}$

B. $((2^{32} - 102) \times 2^{16} - 256) \times 2^{16}$

C. $((2^{32} - 256) \times 2^{16} - 102) \times 2^{16}$ — Correct Option

**Solution :**
(c)




- $(2^{32} - 256)$ instruction left after 2-address instruction.
- Number of 1-address instruction = $((2^{32} - 256) \times 2^{16})$.
- Number of 0-address instruction = $((2^{32} - 256) \times 2^{16} - 102) \times 2^{16}$

D. None

QUESTION ANALYTICS

# COA (GATE - 2021) - REPORTS

OVERALL ANALYSIS | COMPARISON REPORT | SOLUTION REPORT

ALL(17) | CORRECT(0) | INCORRECT(0) | SKIPPED(17)

**Q. 11** Solution Video | Have any Doubt ?

Consider two level cache hierarchies with $L_1$ and $L_2$ cache. Programs refer memory 1000 times out of which 40 misses are in $L_1$ cache and 10 misses are in $L_2$ cache. If the miss penalty of $L_2$ is 200 clock cycles, hit time of $L_1$ is 1 clock cycle, and hit time of $L_2$ is 15 clock cycles, the average memory access time is (in clock cycles (cc)).

A 2.3

B 3.6 — Correct Option

**Solution :**
(b)

$$L_1 \text{ miss rate} = \frac{40}{1000} = 4\%$$

$$L_2 \text{ miss rate (we need to take local miss rate)} = \frac{10}{40} = 25\%$$

Where,
Average access time = Hit time ($L_1$) + Miss rate ($L_1$)
Miss rate ($L_1$) = Hit time ($L_2$) + Miss rate ($L_2$) × Miss penalty
Average access time = 1 + 4% [15 cc + 25% × 200 cc]
= 1 + 0.04[15 cc + 50 cc]
= 3.6 cc

C 4.2

D 5.8

QUESTION ANALYTICS

**Q. 12** Solution Video | Have any Doubt ?

A set associative cache consists of 128 lines divided into 8 lines set. If main memory (MM) contains 4 k blocks of 1024 words each, then the size of set, tag and word bits are respectively.

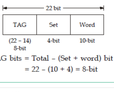
A (5, 7, 10)

B (4, 8, 10) — Correct Option

**Solution :**
(b)

$$\text{Number of sets} = \frac{128}{8} = 2^4 = 4 \text{ bits}$$

$$\text{Number of blocks in MM} = 4k = 2^{12}$$
$$\text{Total MM size} = 2^{12} \times 1024 \text{ words}$$
$$= 2^{12} \times 2^{10} \text{ words} = 2^{22} \text{ words}$$




TAG bits = Total – (Set + word) bit
= 22 – (10 + 4) = 8-bit

C (8, 4, 10)

D (4, 9, 10)

QUESTION ANALYTICS

**Q. 13** Solution Video | Have any Doubt ?

Consider a direct mapped cache of size 32 kB with block size 32 bytes. The CPU generates 32 bit addresses. The number of bits needed for cache indexing and the number of tag bits are respectively.

A 10, 17

B 10, 22

C 15, 17 — Correct Option

**Solution :**
(c)

$$\text{Size of cache} = 32 \text{ kB}$$
$$= 32 \times 2^{10} \text{ byte}$$
$$= 2^5 \times 2^{10} \text{ byte}$$
$$= 2^{15} \text{ byte} \Rightarrow 15 \text{ bits}$$
$$\text{Size of tag} = 32 - 15 = 17 \text{ bits}$$
$$\text{Cache indexing size} = 10 \text{ bits}$$

D 5, 17

QUESTION ANALYTICS

**Q. 14** Solution Video | Have any Doubt ?

A program consists of mainly different types of instructions. The table for instruction type, cycle per instruction (CPI) and frequency of such instructions in the program is given below:

| Type | CPI | Frequency(%) |
|---|---|---|
| ALU | 1 | 35 |
| Branch | 2 | 12 |
| Load/Store | 3 | 28 |
| Memory referring | 4 | 25 |

Then the average CPI of the program is _____.

2.43 (2.40 - 2.50) — Correct Option

**Solution :**
2.43 (2.40 - 2.50)

Average CPI = $\Sigma$CPI$_i$ × Frequency$_i$(%) (where $i$ = 1, 2, 3, 4)
= 1 × 0.35 + 2 × 0.12 + 3 × 0.28 + 4 × 0.25
= 0.35 + 0.24 + 0.84 + 1.0 = 2.43

QUESTION ANALYTICS

**Q. 15** Solution Video | Have any Doubt ?

The number of memory chips of size 1 K × 4 bits required to build a memory bank of size 16 K × 8 bits is _____.

32 — Correct Option

**Solution :**
32
Size of memory is defined as $2^n \times m$ bits, where 'm' is number of data lines in, 'n' is number of address lines.
1 K byte of memory means 1024 bytes of memory

$$\text{Size of memory required} = 16K \times 8 \text{ bits} = 16 \times 1024 \times 8 \text{ bits}$$
$$\text{Size of given chip} = 1 \text{ K} \times 4 \text{ bits} = 1 \times 1024 \times 4 \text{ bits}$$
$$\text{Number of memory chips required,}$$
$$= \frac{16 \times 1024 \times 8}{1 \times 1024 \times 4} = 32 \text{ chips}$$

QUESTION ANALYTICS

**Q. 16** FAQ | Solution Video | Have any Doubt ?

Which of the following statements are not correct?

A In memory-mapped I/O, the CPU can manipulate I/O data residing in interface register that are used to manipulate memory words. — Correct Option

B The isolated I/O method isolates memory and I/O address so that memory address range is not affected by interface address assignment

C In asynchronous serial transfer of data, the two units share a common clock — Correct Option

D In synchronous serial transmission of data, the two units have different clocks. — Correct Option

YOUR ANSWER - NA | CORRECT ANSWER - a,c,d | STATUS - SKIPPED

**Solution :**
(a, c, d)
Memory mapped I/O: This configuration uses common bus and common control signals but unique address space.

QUESTION ANALYTICS

**Q. 17** Solution Video | Have any Doubt ?

Consider the following statements regarding 'Addressing modes':

A To access constant value immediate addressing mode is used. — Correct Option

B Static variables are using direct addressing mode — Correct Option

C Pointers are implemented using indirect addressing mode. — Correct Option

D Arrays are implemented using implied addressing mode.

YOUR ANSWER - NA | CORRECT ANSWER - a,b,c | STATUS - SKIPPED

**Solution :**
(a, b, c)
Arrays are implemented using Based index addressing mode.

QUESTION ANALYTICS