TABLE OF CONTENTS

1. Syllabus

2. Mapping of Program Outcomes with Instructional Objectives

3. Mapping of Program Educational Objectives with Program Outcomes

4. Session plan

5. Laboratory policies & Report format.

6. Evaluation sheet

7. Each experiment should be prefixed with prelab questions with answer key and suffixed with post lab questions with answer key.

8. Projects.

Syllabus

EE 0313	INTEGRATED CIRCUITS LAB	L	T	P	C
	Prerequisite	0	0	3	2
	EE0305				

PURPOSE
To acquire skills of designing and testing integrated circuits

INSTRUCTIONAL OBJECTIVES
1. Analyze and design various applications of Op-Amp
2. Design and construct waveform generation circuits
3. Design timer and analog and digital circuits using op amps.
4. To design combinational logic circuits using digital IC's

LIST OF EXPERIMENTS
1. Operational Amplifiers (IC741)-Characteristics and Application.
2. Waveform Generation using Op-Amp (IC741).
3. Applications of Timer IC555.
4. Design of Active filters.
5. Study and application of PLL IC's
6. Design of binary adder and subtractor.
7. Design of counters.
8. Study of multiplexer and demultiplexer /decoders.
9. Implementation of combinational logic circuits**.**
10. Study of DAC and ADC
11. Op-Amp voltage Regulator- IC 723

TOTAL

REFERENCE
Laboratory Manual

Course designed by	Department of Electrical and Electronics Engineering										
Program outcomes	a	b	c	d	e	f	g	h	i	j	k
	X	X	X		X			X			
Category	General (G)		Basic Sciences (B)		Engineering Sciences and Technical Arts(E)		Professional Subjects(P)				
							X				
Broad area (for 'P'category)	Electrical Machines		Circuits and Systems		Electronics		Power System				
			X		X						
Staff responsible for preparing the syllabus	Mrs.R.Uthra										
Date of preparation	December 2006										

Mapping of Course Outcomes with Instructional Objectives

Mapping of Program Instructional Objectives Vs Program Outcomes

Program Outcomes	Program Instructional objectives			
	To design various types of amplifier using Op-amp	To design waveform generation circuits	To design basic timer and analog and digital circuits	To design simple logic circuits using digital ICs.
a).An ability to apply knowledge of mathematics, science, and engineering.	X	X	X	X
b). An ability to design and conduct experiments, as well as to analyze and interpret results.	X	X	X	X
c).An ability to design a system, component, or process to meet desired needs within realistic constraints such as economic,environmental,social, political, ethical, health and safety, manufacturability, and sustainability.	X	X	X	
e).An ability to identify, formulate, and solve engineering problems	X	X	X	X
h).The broad education necessary to understand the impact of engineering solutions in a global perspective	X	X	X	X

Mapping of Program Educational Objectives with Program Outcomes

Mapping of Program Educational Objectives Vs Program Outcomes

PROGRAM EDUCATIONAL OBJECTIVES

1. Graduates are equipped with the fundamental knowledge of Mathematics, Basic sciences and Electrical and Electronics Engineering.
2. Graduates learn and adapt themselves to the constantly evolving technology by pursuing higher studies.
3. Graduates are better employable and achieve success in their chosen areas of Electrical and Electronics Engineering and related fields.
4. Graduates are good leaders and managers by effectively communicating at both technical and interpersonal levels.

The student outcomes are linked with the program educational objectives as shown below.

PROGRAM OUTCOMES (a–k OUTCOMES)	PROGRAM EDUCATIONAL OBJECTIVES			
	1	**2**	**3**	**4**
(a) an ability to apply knowledge of mathematics, science, and engineering	x			
(b) an ability to design and conduct experiments, as well as to analyze and interpret data	x			
(c) an ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability			x	
(d) an ability to function on multidisciplinary teams			x	x
(e) an ability to identify, formulate, and solve engineering problems			x	
(f) an understanding of professional and ethical responsibility			x	
(g) an ability to communicate effectively in both verbal and written form.				x
(h) the broad education necessary to understand the impact of engineering solutions in a global perspective.		x		
(i) a recognition of the need for, and an ability to engage in life-long learning		x		
(j) a knowledge of contemporary issues		x		
(k) an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.		x	x	

Academic Course Description
SRM University, Kattankulathur
Faculty of Engineering and Technology
Department of Electrical and Electronics Engineering

COURSE : EE0313

TITLE : INTEGRATED CIRCUITS LAB

CREDIT : 02

LOCATION : Electronics Lab ESB223

PREREQUISITES COURSES : EE0305 - Linear Integrated Circuits

EE0307 – Digital Systems

PREREQUISITIES BY TOPIC : Basics of Op-Amps, Timers, Basic logic

gates, Boolean functions**.**

Outcomes
Students who have successfully completed this course

Instructional Objective	Program outcome
The students will be able to: • Analyze and design various applications using Op-amp. • Design and construct waveform generation circuits. • Design timer, analog and digital circuits using op amps. • Design combinational logic circuits using digital ICs.	a).An ability to apply knowledge of mathematics, science, and engineering b). An ability to design and conduct experiments, as well as to analyze and interpret results. c).An ability to design a system, component, or process to meet desired needs within realistic constraints such as economic,environmental,social, political, ethical, health and safety, manufacturability, and sustainability. e).An ability to identify, formulate, and solve engineering problems h).The broad education necessary to understand the impact of engineering solutions in a global perspective

Text book(s) and/or required materials:

1. Linear Integrated Circuits – Roy Choudhary
2. Digital Systems – Morris Mano
3. Ramakant A.Gayakwad, "Op-Amps and Linear Integrated Circuits: Lab Solutions Manual
4. *pulse and digital circuits lab manual PDF*

Web Resources:

1. www.electronics-lab.com
2. ebookee.com-integrated circuits

Professional component:

General   - 0%
Basic Sciences   - 0%
Engineering sciences & Technical arts   - 0%
Professional subject   - 100%

SESSION PLAN:

WEEK	NAME OF THE EXPERIMENT	REFERENCE	OBJECTIVE
I	Op-Amp Characteristics	Op-Amps and Linear Integrated Circuits: Lab Manual "Ramkant.A.Gayakwad	Analyze and design various applications of op-amp
II	Op-Amp application		
III	Waveform generating circuits		Design and construct waveform generation circuits
IV	Active Filters		
V	Application of 555 timer		Design timer, analog and digital circuits using opamps.
VI	DAC and ADC		
VII	Characteristics of PLL		
VIII	Voltage Regulator		
IX	Verification of logical expression and flip flops	Pulse and digital circuits lab manual	To design combinational logic circuits using digital ICs
X	Adders and subtractors		

9

XI	Multiplexer and Demultiplexer	PDF	
XII	Counters		

Course Learning Outcome:

This course provides the foundation education in electric circuit analysis and design. Through lecture, laboratory, and out-of-class assignments, students are provided learning experience that enable them to:	Correlates to program outcome		
	H	**M**	**L**
Design basic application circuits using op-amp.	**H**		
Understand and implement the working of basic digital circuits		**M**	

H: high correlation, M: medium correlation, L: low correlation

EVALUVATION METHOD:

- Prelab Test   -   10%
- Inlab Performance   -   30%
- Postlab Test   -   10%
- Attentance   -   5%
- Record   -   20%
- Final Exam   -   25%
- Total   -   100%

LABORATORY POLICIES AND REPORT FORMAT:

1. **Lab reports should be submitted on A4 paper.** Your report is a professional presentation of your work in the lab. Neatness, organization, and completeness will be rewarded. Points will be deducted for any part that is not clear.
2. The lab reports will be written individually. Please use the following format for your lab reports.

10

a. **Cover Page:** Include your name, Subject Code, Subject title, Name of the university.
b. **Evaluation Sheet: Gives** your internal mark split –up.
c. **Index Sheet:** Includes the name of all the experiments.
d. **Experiment documentation:** It includes experiment name, date, objective, circuit diagram, simulated circuit and verified outputs.
e. **Prelab and Postlab question** should be retyped in the end of every cycle**.**

3. Your work must be original and prepared independently. However, if you need any guidance or have any questions or problems, please do not hesitate to approach your staff in charge during office hours. The students should follow the dress code in the Lab session.

4. Labs will be graded as per the following grading policy:

   - Prelab Test   -   10%
   - Inlab Performance   -   30%
   - Postlab Test   -   10%
   - Attentance   -   5%
   - Record   -   20%
   - Final Exam   -   25%
   - Total   -   100%

5. **Reports Due Dates**: Reports should be submitted at the end of each cycle. A late lab report will have 20% of the points deducted for being one day late. If a report is 3 days late, a grade of 0 will be assigned.

6. **Systems of Tests**: Regular laboratory class work over the full semester will carry a weightage of 75%. The remaining 25% weightage will be given by conducting an end semester practical examination for every individual student. Prelab test is conducted at the beginning of each cycle as a viva-voce and the post lab test is conducted as written test during the permission of report.

LAB EXPERIMENT

- Prelab and Postlab questions for each experiment with answer key
- Evaluation sheet for each experiment

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SRM UNIVERSITY, Kattankulathur – 603203.

Title of Experiment :	
Name of the candidate :	
Register Number :	
Date of Experiment :	
Date of submission **:**	

S.No:	Marks split up	Maximum Marks (50)	Marks Obtained
1	Attendance	5	
2	Preparation of observation/record	10	
3	Pre viva questions	5	
4	Execution of experiment	15	
5	Calculation/evaluation of result	10	
6	Post viva questions	5	

Staff Signature

1. Op amp Characteristics

Pre Lab Questions:
1.   **State the ideal characteristics of Op-amp.**

i) Open loop gain, Aol = ∞
ii) Input impedance, Ri = ∞
iii) Output Impedance, Ro = 0
iv) Zero Offset, Vo = 0
v) Bandwidth, BW = ∞

2.   **Why differential amplifier is used as an input stage of IC op-amp?**

The differential amplifier eliminates the need for an emitter bye-pass capacitor. So, differential amplifier is used as an input stage in op-amp ICs

3.   **What does operational amplifier refers to?**

Operational amplifier refers to an amplifier that performs a mathematical operation. A typical op-amp is a DC amplifier with a very high voltage gain, very high input impedance and very low output impedance.

4.   **What causes slew rate?**
The rate at which internal or external capacitance of Op-amp changes causes slew rate. Also slew rate is caused by current limiting and saturation of internal stages of op-amp where a high frequency, large – amplitude signal is applied.

5.   **Draw the Pin diagram of IC 741.**
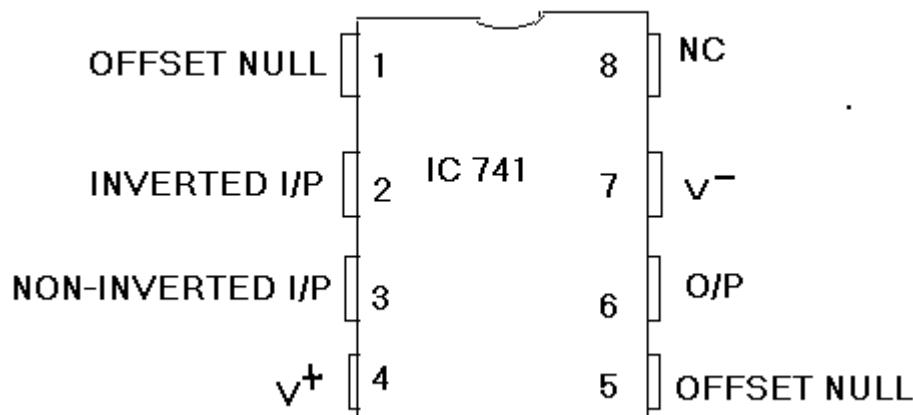
1. CHARACTERISTICS OF OP-AMP

AIM:

To measure the following parameters of op-amp

1. Input bias current
2. Input offset current
3. Input offset voltage
4. Slew rate

APPARATUS REQUIRED:

S.No.	APPARATUS	TYPE	RANGE	QUANTITY
1)	Op-Amp	μA741		1
2)	Resistors		4.7K, 100K, 1M	1
3)	Capacitors		0.01μF	1
4)	Signal Generator			1
5)	CRO			1
6)	Dual power supply			1
7)	Bread Board			1
8)	Connecting wires			

THEORY:

Input bias current: The inverting and noninverting terminals of an op-amp are actually two base terminals of transistors of a differential amplifier. In an ideal op-amp it is supported that no current flows through these terminals. However, practically a small amount of current flows through these terminals which is on the order of nA (typical and maximum values are 80 and 1500nA) in bipolar op-amps and pA for FET op-amps. Input bias current is defined as the average of the currents entering into the inverting and noninverting terminals of an op-amp. To compensate for bias currents a compensating resistor R_{comp} is used. Value of R_{comp} is parallel combination of the resistors connected to the inverting terminal. Input bias current $I_B = \dfrac{(I_{B1} + I_{B2})}{2}$, where I_{B1} and I_{B2} are the base bias currents of the op-amp.

Input offset current: The bias currents I_{B1} and I_{B2} will not be equal in an op-amp. Input offset current is defined as the algebraic difference between the currents into the inverting and non-inverting terminals. $I_{os} = |I_{B1} - I_{B2}|$, Typical and maximum values of input offset current are 20nA and 200nA.

Input offset voltage: Even if the input voltage is zero, output voltage may not be zero. This is because of the circuit imbalances inside the op-amp. In order to compensate this, a small voltage should be applied between the input terminals. Input offset voltage is

15

defined as the voltage that must be applied between the input terminals of an op-amp to nullify the output voltage. Typical and maximum values of input offset voltage are 2mV and 6mV.

Slew rate: Slew rate is the rate of rise of output voltage. It is the measure of fastness of op-amp. It is expressed in V/μsec. If the slope requirements of the output voltage of the op-amp are greater than the slew rate, distortion occurs. Slew rate is measured by applying a step input voltage.

PROCEDURE:

a) Input Bias Current
1. Connect the circuit as shown in Fig.1.1.
2. Measure the output voltage from which the inverting input bias current can be calculated as $I_B^- = Vo/R_f$.
3. Connect the circuit as shown in Fig.1.2.
4. Measure the output voltage from which the non-inverting input bias current can be calculated as $I_B^+ = Vo/R_f$.
5. Average of magnitude of both I_B^- and I_B^+ gives the input bias current.

b) Input Offset Current
1. Connect the circuit as shown in Fig.1.3.
2. Measure the output voltage using multimeter.
3. Calculate the offset current as $I_{os} = V_o/R_f$.

c) Input Offset Voltage
1. Connect the circuit as shown in Fig.1.4.
2. Measure the output voltage using multimeter
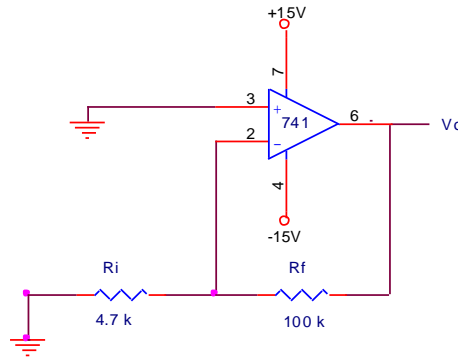3. Calculate offset voltage as $V_{os} = V_o / (1 + R_f / R_1)$.

d) Slew Rate
1. Connect the circuit as shown in Fig.1.5.
2. Give square wave input from the signal generator so that the output is a square wave at 1kHz.
3. Increase the frequency slowly until the output is just barely a triangular wave.
4. Calculate slew rate as $SR = (\Delta V / \Delta t)$.
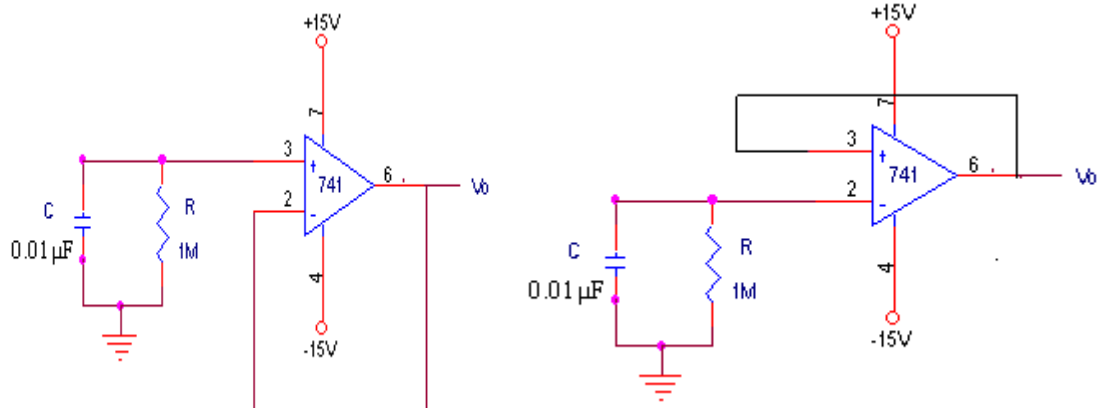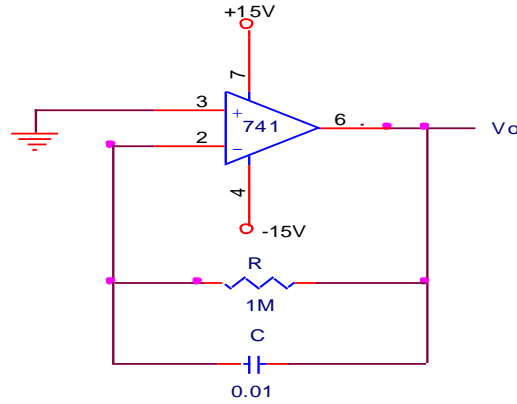
PIN DIAGRAM:
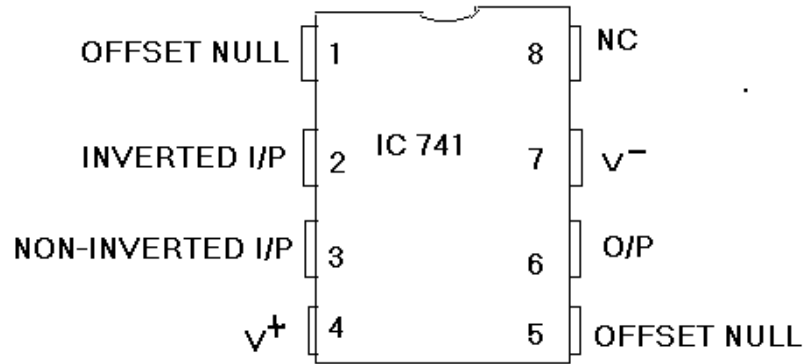
CIRCUIT DIAGRAM:

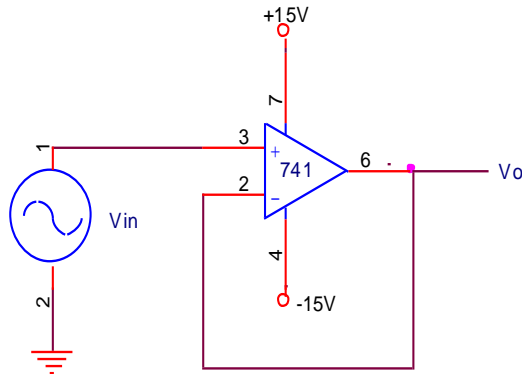To measure input offset voltage

To measure input bias current

To measure input offset current

To measure slew rate

TYPICAL VALUES OF ELECTRICAL CHARACTERISTICS OF μA741:

Input bias current   =   80-500nA
Input offset current   =   20-200nA
Input offset voltage   =   1-5mV
Slew rate   =   <0.5 V/μs

RESULT:

       The input bias current, input offset current, input offset voltage and slew rate of the op-amp were determined.

Input offset voltage   = …….. mV
Input bias current   = …….. A
Input offset current   = ...…... A
Slew rate   = …….. V/μs.

18

Post Lab Questions:
1.   **What is input bias current?**

The average of the currents entering the negative input (I_B^-) and positive input (I_B^+) of an op-amp is called input bias current(I_B)
The equation is
$$I_B = I_B^+ - I_B^- / 2$$

2. Why do we use R_{comp} resistor?

In a bipolar op-amp circuit, even when the input is zero, the output will not be zero. This is due to effect of input bias current. This effect can be compensated by using compensation resistor $R_{comp,}$ where

3. **What is thermal drift?**

In an op-amp the bias current, offset current and off set voltage changes with change in temperature. Offset current drift is measured in nA/ ^{0}C and offset voltage drift is measured in mV/ ^{0}C. These indicate the change in offset current or voltage for each degree Celsius change in temperature. Forced air cooling may be used to stabilize the ambient temperature

4. **Why is IC741 op-amp not used for high frequency applications?**

Op-amp IC741 has very low slew rate (0.5V/µS) and therefore cannot be used for high frequency applications.

5.   **What is unity gain circuit?**

Voltage follower is called unity gain circuit. The circuit does not amplify and provides constant gain of unity.

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Title of Experiment :	
Name of the candidate :	
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Date of submission **:**	

S.No:	Marks split up	Maximum Marks (50)	Marks Obtained
1	Attendance	5	
2	Preparation of observation/record	10	
3	Pre viva questions	5	
4	Execution of experiment	15	
5	Calculation/evaluation of result	10	
6	Post viva questions	5	

Staff Signature

2. Op amp Applications

Pre lab Questions :

1. What is a comparator?

A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with known reference voltage at other input. It is basically an Op-amp with output V_{sat} ($\gg V_{cc}$).

2. What is the difference between a basic comparator and ZCD?

Comparator has only one reference voltage whereas ZCD has zero reference voltage.

3. Give the gain expression for inverting and non inverting amplifier.

Inverting Amplifier = -Rf/Ri
Non inverting Amplifier = 1+(Rf/Ri)

4. State some linear and non linear applications of Op-amp.

Linear:
a) Adder
b) Subtractor
c) Instrumentation amplifier
Non linear:
a) Rsctifier
b) Peak detector
c) Clippers and Clampers.

5. Differentiator is also a <u>High pass</u> **filter.**

6. Integrator is also a <u>low pass</u> **filter.**

2. APPLICATIONS OF OP-AMP

AIM:

To demonstrate the use of op-amp as (1) summing amplifier (2) subtractor (3) zero crossing detector and (4) voltage comparator.

APPARATUS REQUIRED:

S.No.	APPARATUS	TYPE	RANGE	QUANTITY
1)	Op-Amp	μA741		1
2)	Resistors		10K, 1K	1
4)	Signal Generator			1
5)	CRO			1
6)	Dual power supply			1
7)	Bread Board			1
8)	Connecting wires			

THEORY:

Summing Amplifier: Op-amp may be used to perform summing operation of several input signals in inverting in inverting and non-inverting mode. The input signals to be summed up are given to inverting terminal or non-inverting terminal through the input resistance to perform inverting and non-inverting summing operations respectively.

Subtractor: The basic difference amplifier can be used as a subtractor. The signals to be subtracted are connected to opposite polarity inputs i.e. in inverting or non-inverting terminals of the op-amp.

Voltage Comparator: A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with output $\pm V_{sat} = (V_{cc})$. If the signal is applied to the inverting terminal of the op-amp it is called inverting comparator and if the signal is applied to non-inverting terminal of the op-amp it is called non-inverting comparator. In an inverting comparator if input signal is less than reference voltage, output will be $+V_{sat}$. When input signal voltage is greater than reference voltage output will be $-V_{sat}$. The vice-versa takes place in non-inverting comparator.

Zero Crossing Detector: Zero crossing comparator (ZCD) is an application of voltage comparator. It converts any time varying signal to square of same time period with amplitude $\pm V_{sat}$. The reference voltage is set as zero volts. When the polarity of the input signal changes, output square wave changes polarity.

Integrator: Integrator is used to integrate the i/p waveform. i.e; $V_O = \int V_{in}\, dt$. Here in the inverting amplifier configuration, the feedback resistor R_f is replaced by capacitor C_f. Integrators are commonly used in wave shaping n/ws, signal generators etc. For proper wave integration, T >> RC. Gain and linearity of the o/p are two advantages

of op-amp integrators. Linearity is due to linear charging of capacitor. Its limitation is for Vin=0 and for low frequencies, $X_{Cf} = \infty$ or the capacitor C_f acts as an open circuit. Therefore the op-amp integrator works as an open loop amplifier and the gain becomes infinity or very high.

Differentiator: Here the output waveform is the derivative of the i/p waveform. In a basic inverting amplifier, if R_1 is replaced by C_1, we get the differentiator. But at high frequencies, the gain of the circuit (Rf/XC1) increases with increase in frequency at the rate of 20dB/decade. This makes the circuit unstable. Also X_{C1} decreases when frequency increases.

PROCEDURE:

    a) **Inverting summing amplifier:**
        1.   Connect the circuit as shown in figure
        2.   Connect batteries for voltage V_1, V_2.
        3.   Measure and note the output voltage and compare it with theoretical value $Vo = -(R_f / R_i) (V_1 + V_2)$

    b) **Subtractor:**
        4.   Connect the circuit as shown in figure
        5.   Measure and note the output voltage and compare it with theoretical value.

    c) **Voltage comparator:**
        6.   Connect the circuit as shown in the figure
        7.   Connect an alternating waveform to the non-inverting input of the op-amp
        8.   Connect a reference voltage source to inverting input of the op-amp
   9.   Plot the input and output waveform.

    d) **Zero crossing detector:**
        10.   Connect the circuit as shown in figure
        11.   Connect the input to a signal generator generating a sin wave with one volt peak to peak at 1kHz.
        12.   Connect the input and output to dual channel CRO and compare the input and output.
        13.   Plot the input and output waveform in a graph.

    e) **Integrator & Differentiator:**
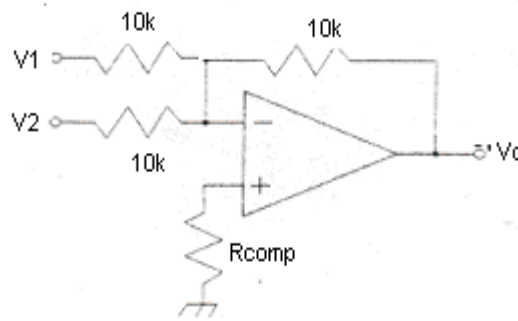   1.   Connections are made as per the diagram.
        2.   Apply an i/p voltage of 1-2Vpp with 1kHz frequency and check the waveform on the CRO.
        3.   Measure the value of V_O by varying the frequency of the i/p signal.
        4.   Calculate gain using the formulae $20 \log (V_O / V_{IN})$.
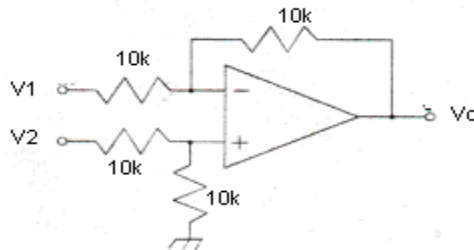
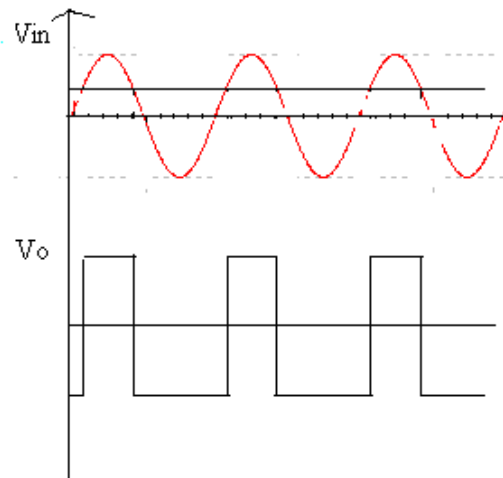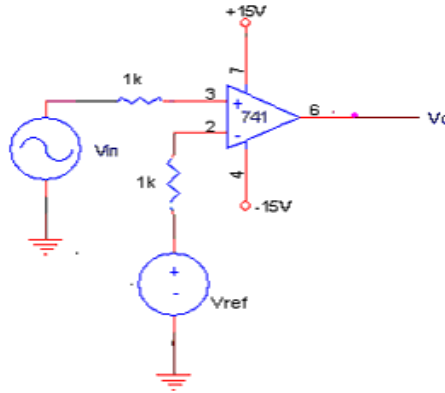**PIN DIAGRAM:**
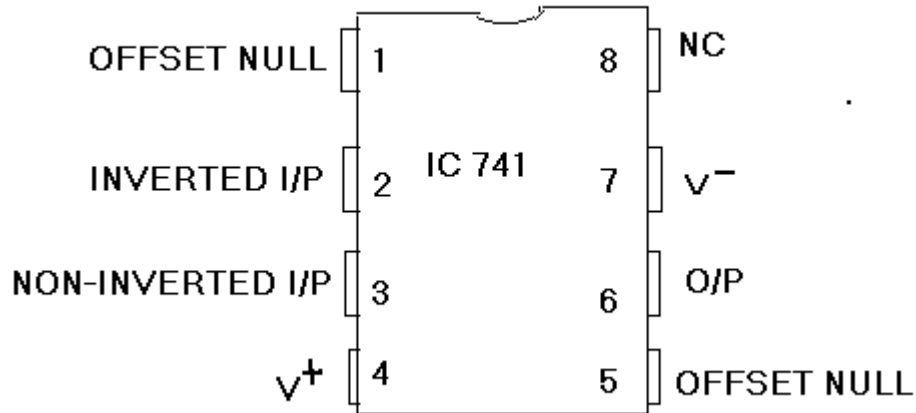
CIRCUIT DIAGRAM:

Summing Amplifier:

S.No.	V1	V2	Theoretical V0=V1+V2	Practical V0
1.	5	3.4	8.4	8.5
2.	10	10	20	21.8

Subtractor:

24

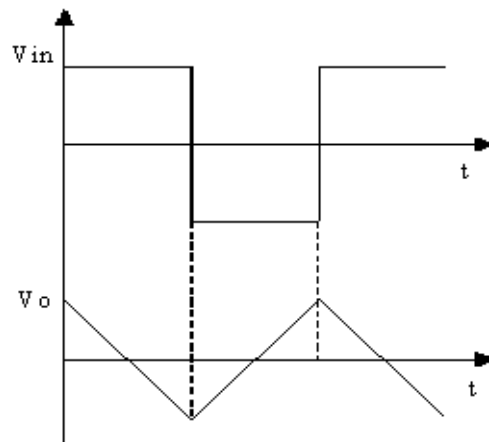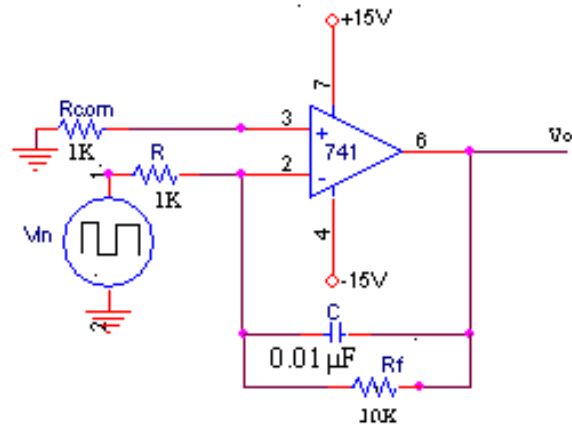| S.No.	V1	V2	Theoretical V0=V1-V2	Practical V0
1.	10	7	3	3.003
2.	10	12	-2	-2.01

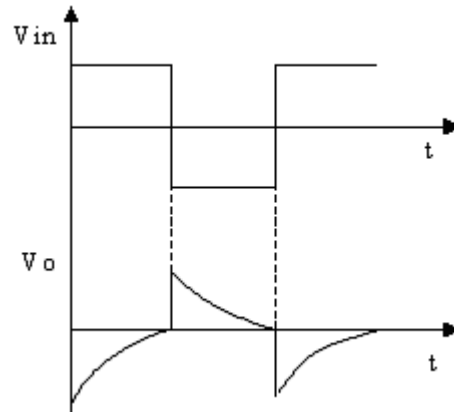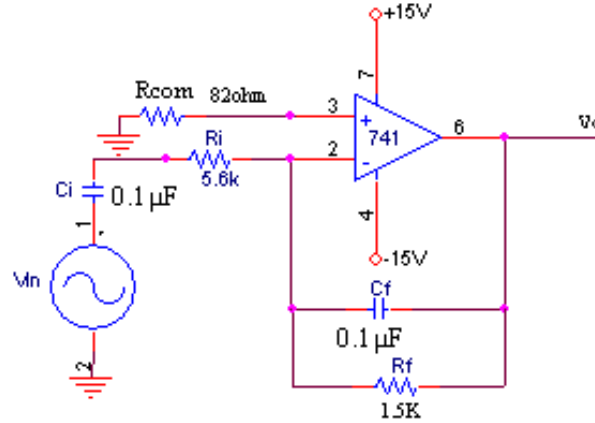**Voltage Comparator:**

Zero Crossing Detector:
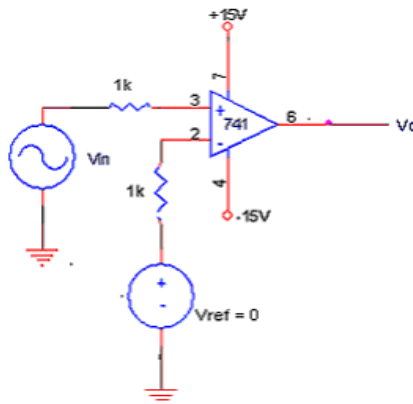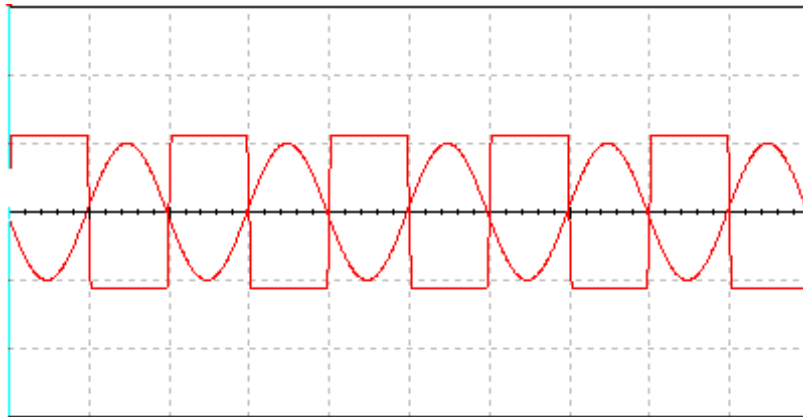
Integrator:

Differentiator:

RESULT:

  Thus, the use of op-amp as summing amplifier, subtractor, voltage comparator, zero crossing detector, integrator, differentiator was studied.

Post Lab Questions:

1.   State some applications of integrator.

    a) Analog computers
    b) ADC
    c) Signal wave shaping circuits.

2.   What are the characteristics of Comparator?

    a) Speed of operation
    b) Accuracy
    c) Compatibility of the output.

3.   List some applications of comparator.

    a) Window detector
    b) Time marker generator
    c) Phase meter
    d) Zero crossing detector

4.   What are the modes in which op-amp is operated with finite gain and infinite gain?

    Open loop mode with infinite gain: Comparator
    Closed loop mode with finite gain: Amplifier

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Title of Experiment	:
Name of the candidate	:
Register Number	:
Date of Experiment	:
Date of submission	**:**

S.No:	Marks split up	Maximum Marks (50)	Marks Obtained
1	Attendance	5	
2	Preparation of observation/record	10	
3	Pre viva questions	5	
4	Execution of experiment	15	
5	Calculation/evaluation of result	10	
6	Post viva questions	5	

Staff Signature

2. Logical Expression

Pre Lab Questions:

1. **Which gates are called Universal gates?**

   NAND and NOR gates are called universal gates because any basic gates can be implemented using these gates.

2. **What is combinational logic?**

   It consists of logic gates whose output at any time is determined directly from the present combinations of the inputs without regards to previous inputs.

3. **What is sequential logic?**

   It uses memory elements in addition to logic gates. Their outputs are function of inputs and state of the memory elements.

4. **What is Flip flop?**

   A Flip flop is a sequential circuit which can maintain the binary state indefinitely as long as power is delivered to the circuit, until directed by an input signal to switch states.

3. VERIFICATION OF LOGICAL EXPRESSION AND FLIP-FLOPS

AIM:
To design a combinational circuit, to implement and verify the given logical expression.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Digital IC trainer kit		1
5.	Connecting wires		As required

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THEORY:

a)Logical Expression: A literal is the primed or unprimed variable. When a Boolean function is implemented with logic gates, each literal in the function designates an input to a gate and each term is implemented with a gate. The minimization of number of literals and the number of terms results in a circuit with less equipments. It is not always possible to minimize both simultaneously. Usually further criteria must be available. The number of literals in a Boolean function can be minimized by algebraic manipulation. The only method available is cut and try procedure employing the postulates, the basic theorems and other manipulation method which becomes familiar with use.

b)Flip-flops:

RS Flip Flop:
The clocked RS flip flop consists of NAND gates and the output changes its state with respect to the input on application of clock pulse. When the clock pulse is high the S and R inputs reach the second level NAND gates in their complementary form.   The Flip Flop is reset when the R input high and S input is low. The Flip Flop is set when the S input is high and R input is low. When both the inputs are high the output is in an indeterminate state.

JK Flip Flop:
The indeterminate state in the SR Flip-Flop is defined in the JK Flip Flop. JK inputs behave like S and R inputs to set and reset the Flip Flop. The output Q is ANDed with K input and the clock pulse, similarly the output Q' is ANDed with J input and the Clock pulse. When the clock pulse is zero both the AND gates are disabled and the Q and Q' output retain their previous values. When the clock pulse is high, the J and K inputs reach the NOR gates. When both the inputs are high the output toggles continuously. This is called Race around condition and this must be avoided.

T Flip Flop:
This is a modification of JK Flip Flop, obtained by connecting both inputs J and K inputs together. T Flip Flop is also called Toggle Flip Flop.
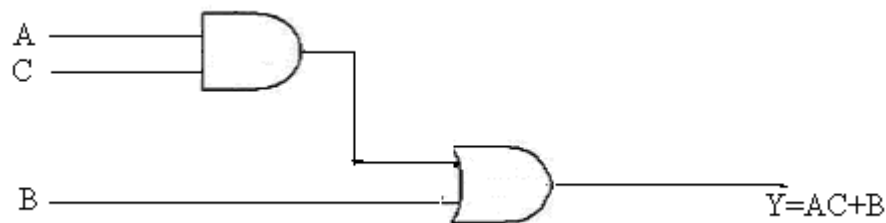
31

BOOLEAN LAWS:

1) $A + 0 = A$
2) $A + 1 = 1$
3) $A \cdot 0 = 0$
4) $A \cdot 1 = A$
5) $A + A = A$
6) $A + \overline{A} = 1$
7) $A \cdot A = A$
8) $A \cdot \overline{A} = 0$
9) $\overline{\overline{A}} = A$
10) $A + AB = A$
11) $A + \overline{A} B = A + B$
12) $(A + B)(A + C) = A + BC$

DE-MORGAN'S THEOREM:

1) $\overline{AB} = + \overline{B}$
2) $\overline{A + B} = \cdot \overline{B}$

MINIMIZATION OF EXPRESSION:

AB + A(B+C) + B (B+C)

$=$ AB + AB + AC + BB + BC
$=$ AB + AB + AC + B + BC
$=$ AB + AB + AC + B (1+C) [1+C=1]
$=$ AB + AB + AC + B [A+A = A]
$=$ AB + AC + B
$=$ B (A+1) + AC [1+A=1]
$=$ B+AC

LOGICAL DIAGRAM:

$Y = AC + B$

TRUTH TABLE:

A	B	C	AC	AC+B
0	0	0	0	0
0	0	1	0	0
0	1	0	0	1
0	1	1	0	1
1	0	0	0	0
1	0	1	1	1
1	1	0	0	1
1	1	1	1	1

PROCEDURE:

a) Logical expression:

  1. Minimize the given expression using Boolean laws or K-map technique.
  2. Design the expression using combinational circuit as shown in figure
  3. Verify the output

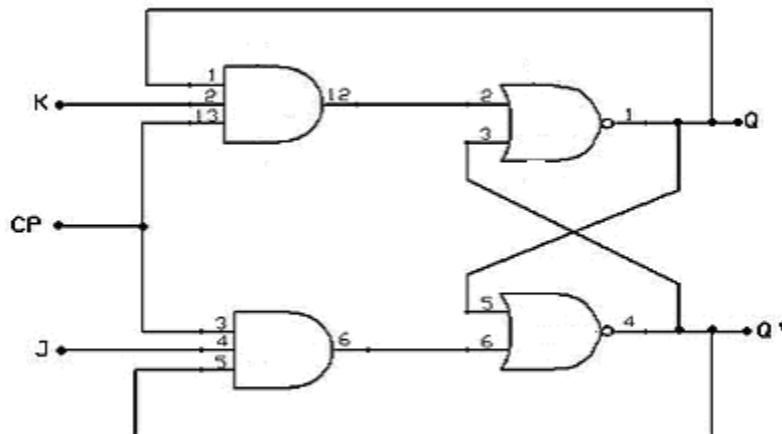**b) Flip-Flops:**

  1. Connections are given as per the circuit diagrams.

  2. For all the ICs 7th pin is grounded and 14th pin is given +5 V supply.

  3. Apply the inputs and observe the status of all the flip flops.

CIRCUIT DIAGRAM:

a) RS Flip-flop:
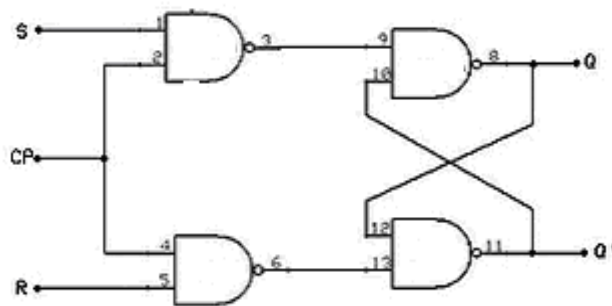
CHARACTERISTIC TABLE:

S.No:	INPUT		Q'	Q
	S	**R**		
1	**0**	**0**	**0**	**0**
2	**0**	**0**	**1**	**1**
3	**0**	**1**	**0**	**0**
4	**0**	**1**	**1**	**0**
5	**1**	**0**	**0**	**1**
6	**1**	**0**	**1**	**1**
7	**1**	**1**	**0**	**X**
8	**1**	**1**	**1**	**X**

b) JK Flip-flop:

CHARACTERISTIC TABLE:

S.No:	INPUT		Q'	Q
	J	**K**		
1	**0**	**0**	**0**	**0**
2	**0**	**0**	**1**	**1**
3	**0**	**1**	**0**	**0**
4	**0**	**1**	**1**	**0**
5	**1**	**0**	**0**	**1**
6	**1**	**0**	**1**	**1**
7	**1**	**1**	**0**	**1**
8	**1**	**1**	**1**	**0**

34
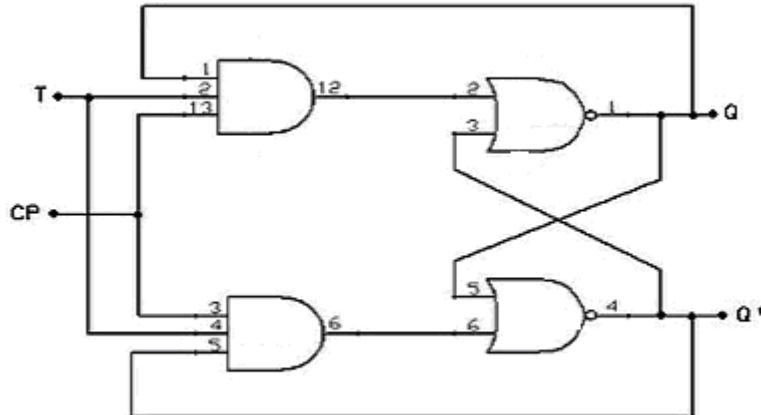
c) T Flip-flop:

CHARACTERISTIC TABLE:

S.No:	INPUT T	Q'	Q
1	0	0	0
2	0	1	0
3	1	0	1
4	1	1	0

RESULT:

    A circuit was designed to implement the given logical expression and flip – flops and the output was verified.

Post Lab Questions:

1. **What are the characteristics of a clocked R-S flip flop?**

    RS Flip flop has 2 inputs. The cross coupled connection from the output of one gate to the input of other gate constitutes a feedback path.

2. **Bubbled OR gate is equal to** NAND gate

3. **Bubbled AND gate is equal to** NOR gate

4. **What is the difference between Latch and Flip flop?**

    Latches are level sensitive, flip flops are edge sensitive. Flip flops changes its output only at times determined by clock signal. Latches changes output any time independent of clock signal.

5. **How can you convert SR flip flop to JK flip flop?**

    By giving the feed back we can convert, i.e Q=>S and Q=>R. Hence the S and R inputs will act as J and K respectively.

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Title of Experiment	:
Name of the candidate	:
Register Number	:
Date of Experiment	:
Date of submission	**:**

S.No:	Marks split up	Maximum Marks (50)	Marks Obtained
1	Attendance	5	
2	Preparation of observation/record	10	
3	Pre viva questions	5	
4	Execution of experiment	15	
5	Calculation/evaluation of result	10	
6	Post viva questions	5	

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4. Adders and Subtractors

Pre Lab Questions:

1. **Derive the logical expression for full adder using K-map.**

K-Map for SUM:

A \ BC	00	01	11	10
0		1		1
1	1		1	

SUM = A'B'C + A'BC' + ABC' + ABC

K-Map for CARRY:

A \ BC	00	01	11	10
0			1	
1		1	1	1

CARRY = AB + BC + AC

2. **Derive the logical expression for half adder using K-map.**

K-Map for SUM: K-Map for CARRY:

A \ B	00	01
00		1
01	1	

A \ B	00	01
00		
01		1

SUM = A'B + AB'   **CARRY = AB**

3. **Derive the logical expression for half subtractor using K-map.**

K-Map for DIFFERENCE**:**

A \ B	00	01
00		1
01	1	

DIFFERENCE = A'B + AB'

K-Map for BORROW**:**

A \ B	00	01
00		1
01		

BORROW = A'B

4. **Derive the logical expression for full subtractor using K-map.**

K-Map for DIFFERENCE**:**

A \ BC	00	01	11	10
0		1		1
1	1		1	

Difference = A'B'C + A'BC' + AB'C' + ABC

K-Map for BORROW**:**

A \ BC	00	01	11	10
0		1	1	1
1			1	

Borrow = A'B + BC + A'C

39

4. ADDERS AND SUBTRACTORS

AIM:

To construct the circuits of adder & subtractor and verify their truth table.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Digital IC trainer kit		1
2.	Connecting wires		As required

.

THEORY:

a) Half Adder:

A combinational circuit which performs the addition of two bits is called half adder. The input variables designate the augend and the addend bit, whereas the output variables produce the sum and carry bits.

b) Full Adder:

A combinational circuit which performs the arithmetic sum of three input bits is called full adder. The three input bits include two significant bits and a previous carry bit. A full adder circuit can be implemented with two half adders and one OR gate.

c) Half Subtractor:

A combinational circuit which performs the subtraction of two bits is called half subtractor. The input variables designate the minuend and the subtrahend bit, whereas the output variables produce the difference and borrow bits.

d) Full Subtractor:

A combinational circuit which performs the subtraction of three input bits is called full subtractor. The three input bits include two significant bits and a previous borrow bit. A full subtractor circuit can be implemented with two half subtractors and one OR gate.

PROCEDURE:

a) **Half Adder:**
1. Connect the circuit as per the circuit diagram
2. For various inputs, note the corresponding output.
3. Verify the truth table of half adder.

b)   Full Adder:
   4.   Connect the circuit as per the circuit diagram.
   5.   For various inputs, not the corresponding output.
   6.   Verify the truth table of full adder.

c)   Half Subtractor:
   7.   Connect the circuit as per the circuit diagram
   8.   For various inputs, note the corresponding output
   9.   Verify the truth table of half subtractor

d)   Full Subtractor:
   10.   Connect the circuit as per the circuit diagram
   11.   For various inputs note the corresponding output
   12.   Verify the truth table of full subtractor

CIRCUIT DIAGRAM:
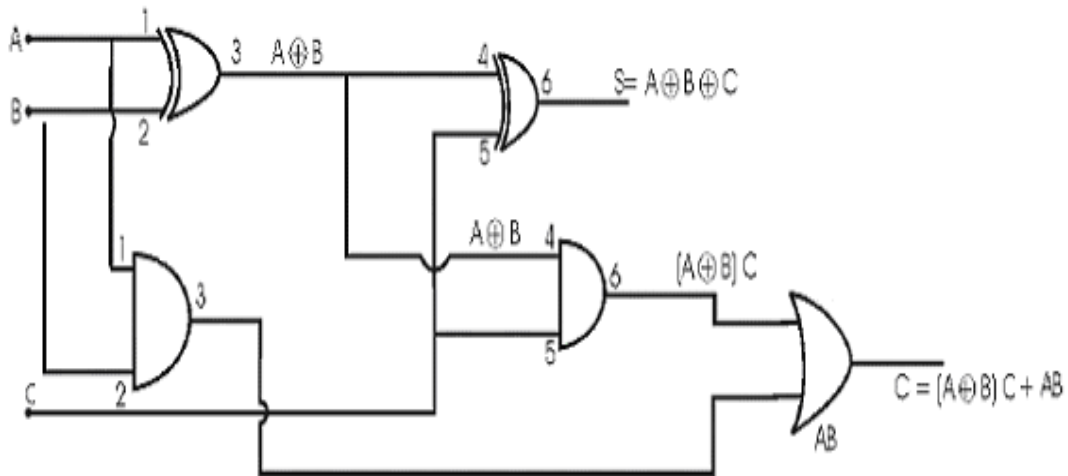
a) Half Adder:

TRUTH TABLE:

S.No:	INPUT		OUTPUT	
	A	**B**	**S**	**C**
1.	0	0	0	0
2.	0	1	1	0
3.	1	0	1	0
4.	1	1	0	1
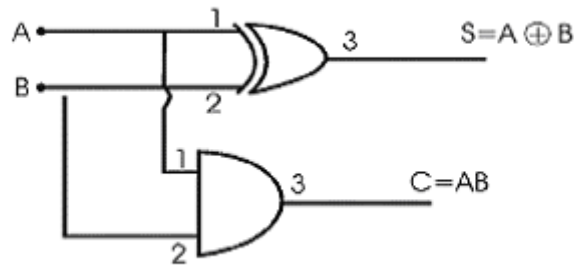
b) Full adder:

TRUTH TABLE:

S.No:	INPUT			OUTPUT	
	A	B	C	SUM	CARRY
1.	0	0	0	0	0
2.	0	0	1	1	0
3.	0	1	0	1	0
4.	0	1	1	0	1
5.	1	0	0	1	0
6.	1	0	1	0	1
7.	1	1	0	0	1
8.	1	1	1	1	1

c) Half Subtractor:

TRUTH TABLE:

S.No:	INPUT		OUTPUT	
	A	B	DIFF	BORR
1.	0	0	0	0
2.	0	1	1	1
3.	1	0	1	0
4.	1	1	0	0
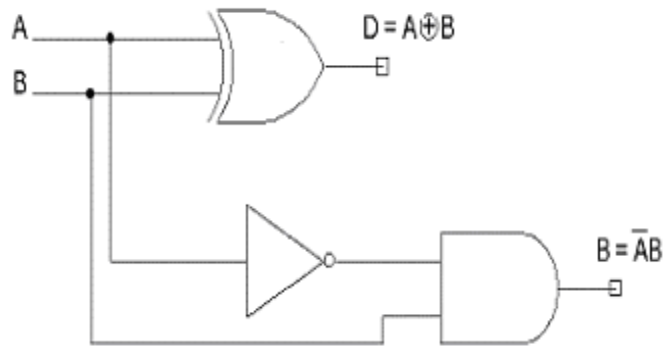
d) Full Subtractor:

TRUTH TABLE:

S.No:	INPUT			OUTPUT	
	A	**B**	**C**	**DIFF**	**BORR**
1.	0	0	0	0	0
2.	0	0	1	1	1
3.	0	1	0	1	1
4.	0	1	1	0	1
5.	1	0	0	1	0
6.	1	0	1	0	0
7.	1	1	0	0	0
8.	1	1	1	1	1
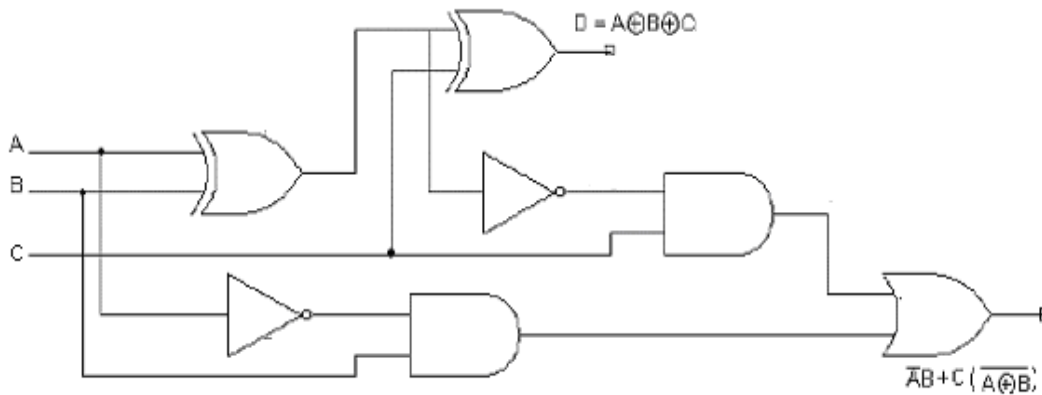
RESULT:

Adders & Subtractors were constructed and their truth tables were verified.

43

Post Lab Questions:

1. **What is half adder?**
   A combinational circuit that performs addition of 2 bits. It consists of 2 inputs and 2 outputs.

2. **What is full adder?**
   A combinational circuit that performs addition of 3 bits. It consists of 3 inputs and 2 outputs.

3. **What are half and full subtractor?**
   Combinational circuit that performs the subtraction of 2 bits is half subtractor and the circuit that performs the subtraction of 3 bits is called full subtractor.

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Name of the candidate	:
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S.No:	Marks split up	Maximum Marks (50)	Marks Obtained
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5. Multiplexer and Demultiplexer

Pre Lab Questions:

1.   What is a multiplexer?

It is a digital circuit which transmits large number of information units through small number of channels.

2.   What is demultiplexer?

It is a logical circuit which receives data in asingle line and transmits it in possible 2^n lines.

3.   Multiplexer is also called data selector**.**

4.   Demultiplexer is also called data distributor**.**

5.   What is the difference between demultiplexer and decoder?

Demultiplexer does not have enable line.

5. MULTIPLEXER AND DEMULTIPLEXER

AIM:
　　　　To construct the circuit of multiplexer and demultiplexer and to study their working.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Digital IC trainer kit		1
5.	Connecting wires		As required

THEORY:
　　　　A multiplexer is a combinational logic circuit, which can select any one of the numbers of inputs and route it to a single output. Multiplexers are available with four, eight and sixteen inputs and a single output. It is also called data selector. The basic multiplexer has several data input lines and a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally, there are 2^n input lines and n selector lines whose bit combinations determine which input is selected. Therefore, multiplexer is 'many into one' and it provides the digital equivalent of an analog selector switch.

　　　　A demultiplexer has a single input and many outputs. The input to a demultiplexer can be routed to any of the output channels. For this reason, a demultiplexer is also known as data distributor. The selection of specific output line is controlled by the values of n selection lines.
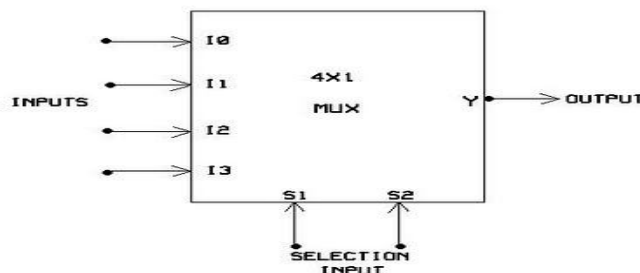
PROCEDURE:
a) Multiplexer:
　　　　1.　　　Connect the circuit as per the circuit diagram.
　　　　2.　　　For various inputs note the corresponding outputs.
　　　　3.　　　Verify the truth table of multiplexer.
b) Demultiplexer:
　　　　1.　　　Connect the circuit as per the circuit diagram.
　　　　2.　　　For various inputs note the corresponding outputs.
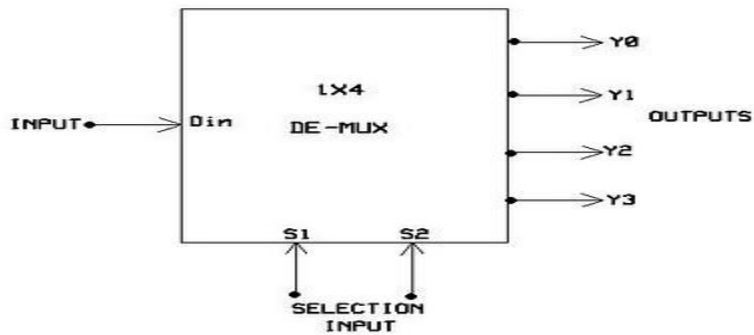　　　　3.　　　Verify the truth table of demultiplexer.

Multiplexer:

TRUTH TABLE:

S.No:	SELECTION INPUT		OUTPUT
	S1	S2	Y
1.	0	0	I_0
2.	0	1	I_1
3.	1	0	I_2
4.	1	1	I_3
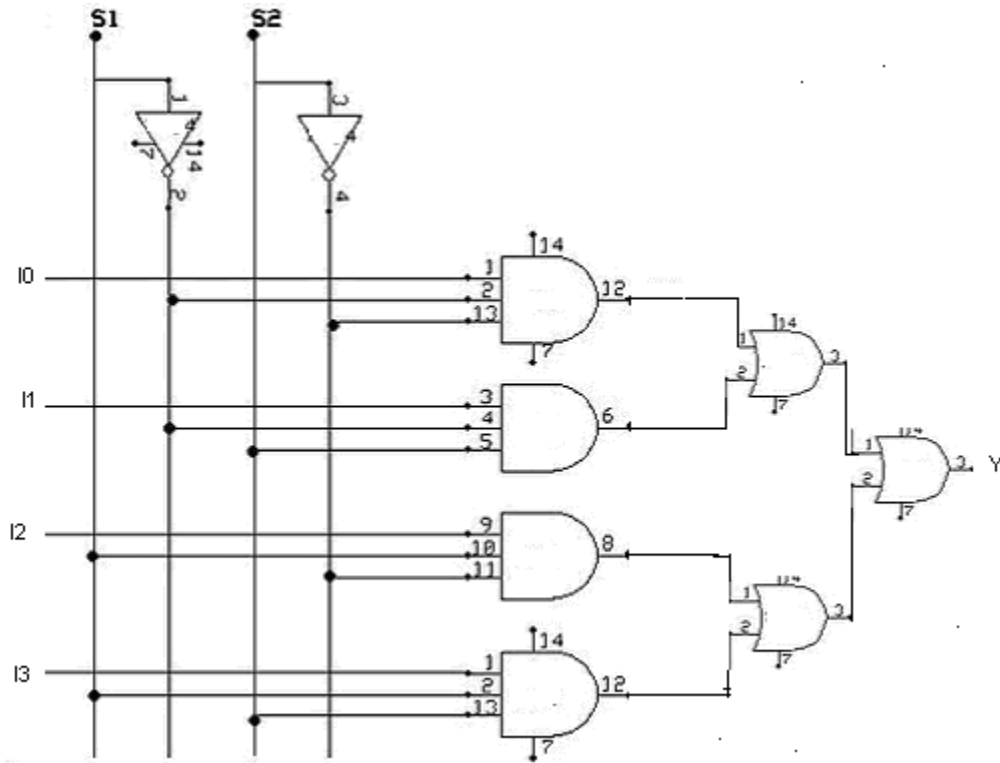
Demultiplexer:

TRUTH TABLE:

S.No:	INPUT			OUTPUT			
	S1	S2	Din	Y0	Y1	Y2	Y3
1.	0	0	0	0	0	0	0
2.	0	0	1	1	0	0	0
3.	0	1	0	0	0	0	0
4.	0	1	1	0	1	0	0
5.	1	0	0	0	0	0	0
6.	1	0	1	0	0	1	0
7.	1	1	0	0	0	0	0
8.	1	1	1	0	0	0	1
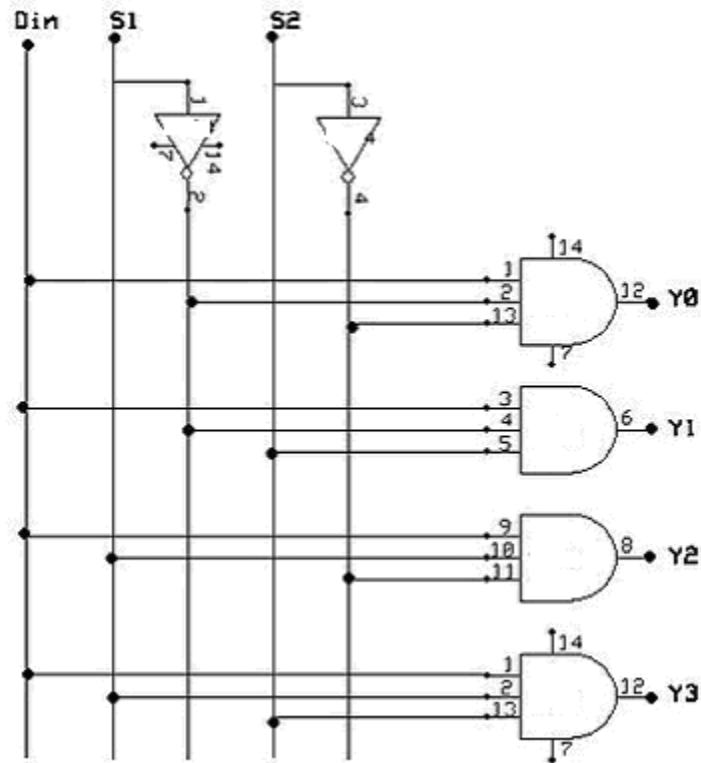
RESULT:

Multiplexer and demultiplexer circuits were constructed and their operations were verified.

Post Lab Questions:
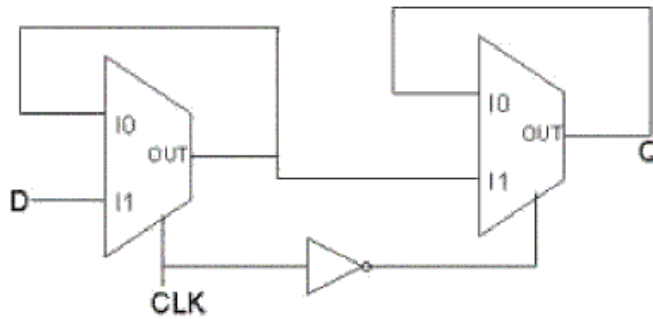
1.   **State some applications of multiplexer and demux.**

        a) Modem
        b) Communication circuits.

2.   **Build a 4:1 mux using only 2:1 mux?**
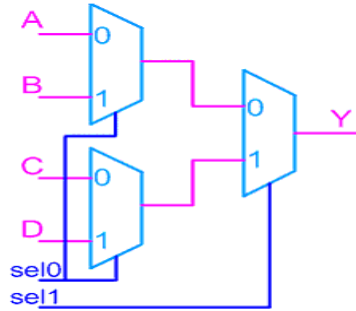
3.   **How to implement a Master Slave flip flop using a 2 to 1 mux?**

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Title of Experiment	:
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4	Execution of experiment	15	
5	Calculation/evaluation of result	10	
6	Post viva questions	5	

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6. Waveform generation circuits

Pre Lab Questions:

1. **What is the basic difference between comparator and Schmitt trigger?**

   A comparator compares the input signal with reference voltage and gives the output whereas Schmitt trigger operates between two reference points LTP and UTP.

2. **State barkhausen criterion.**

   a) Magnitude, $|A_v \beta| = 1$
   b) Phase, $\angle A_v \beta = 0$

4. **What is the merit of regenerative comparator?**

   In regenerative comparator, the feedback enhances the comparator input. The phase difference is not visualized due to positive feedback.

4. **What is an oscillator?**

   An oscillator is basically a positive feedback circuit where a fraction of output voltage Vo is fed back to the input end of the basic amplifier, which is in phase with the signal to the basic amplifier.

5. **Design a Wein bridge oscillator for a frequency of 1KHz.**

   f = 1/2 Π RC
   C = 0.1 μ F
   R = 1/2 Π fC
     = 1/(2*3.14*1*10^3*0.1*10^-6)
     = 628 Ω

6. WAVEFORM GENERATING CIRCUITS

AIM:
To design a schmitt trigger a wien bridge oscillator and to study their operation.

APPARATUS REQUIRED:

S.No.	APPARATUS	TYPE	RANGE	QUANTITY
1)	Op-Amp	µA741		1
2)	Resistors		29K, 1K, 16K, 1.6K	1
3)	Capacitors		0.1µF	1
4)	Signal Generator			1
5)	CRO			1
6)	Dual power supply			1
7)	Bread Board			1
8)	Connecting wires			

THEORY:

Schmitt Trigger

Schmitt trigger is otherwise called regenerative comparator. In this comparator circuit a positive feedback is added. The input voltage Vi triggers the output Vo very time it exceeds certain voltage levels. These voltages are known as upper threshold voltage (V_{UT}) and lower threshold voltage V_{LT}. The difference between

There two threshold voltages ($V_{UT} - V_{LT}$) gives the hysteresis width.

$$V_{UT} = V_{ref} + (R_2 / (R_1 + R_2)) * (V_{sat} - V_{ref})$$

V_{ref} -   applied reference voltage
V_{sat} -   saturation voltage of OP-AMP
R_1, R_2 -   Voltage divider resistances

$$V_{LT} = V_{ref} - (R_2 / (R_1 + R_2)) * (V_{sat} - V_{ref})$$

When input voltage is greater than V_{UT}, output goes to negative saturation and when input voltage is less than V_{LT}, output goes to positive saturation.

Wien bridge Oscillator:

Wien bridge oscillator is one of the most commonly used audio frequency oscillator owing to its simplicity and stability. Wien bridge circuit is connected between the amplifier input terminals and output terminals. The bridge has a series RC network in

53

one arm and a parallel RC network in the adjoining arm. In the remaining two arms of the bridge, resistors R_1 and R_f are connected. The phase angle criterion for oscillation is that the total phase shift around the circuit must be 0°. This conditions occurs only when the bridge is balanced, that is, at resonance. The frequency of oscillation is exactly the resonant frequency of the balanced Wien bridge.

Design of wien bridge oscillator

$$fo \; = \; \frac{1}{2\pi RC} = \frac{0.159}{RC} => (A)$$

Assuming that the resisters are equal in value, and capacitors are equal in value in the reactive leg of the wien bridge. At this frequency the gain required for substained oscillation is given by

Ao -> gain g the op-amp

β -> feed back factor

$$Ao = \frac{1}{3}$$

$$\frac{1+Rf}{R} = 3$$

$$\frac{R_1 + R_f}{R_1} = 3$$

$R_1 + R_f = 3R_1$, $R_f = 2R_1$

Design of Schmitt trigger

Given $V_{UT} = 0.5V$ $V_{LT} = -0.5V$

$$V_{UT} = \frac{R_2}{R_1 + R_2} V_{sat}$$

$$V_{LT} = \frac{R_2}{R_1 + R_2}(-V_{sat})$$

Taking $\pm V_{sat} = \pm 15V$,

$$0.5 = \frac{R_2}{R_1 + R_2}(15V)$$

$$\frac{R_2}{R_1 + R_2} = 30$$

$$\frac{R_2}{R_2} = 29$$

$$= R_1 = 29R_2$$

Taking $R_2 = 1K\Omega$

$R_1 = 29K\Omega$ (set using 100K POT)

PROCEDURE:

a) **Schmitt trigger:**
1. Connect the circuit as shown in diagram
2. See the input sine wave and output from pin.6 in a dual channel, CRO
3. Plot the observed waveforms in a linear graph.
4. Calculate the lower threshold voltage and upper threshold voltage from the plotted graph.
5. Calculate the lower threshold voltage and upper threshold voltage theoretically using the formula.
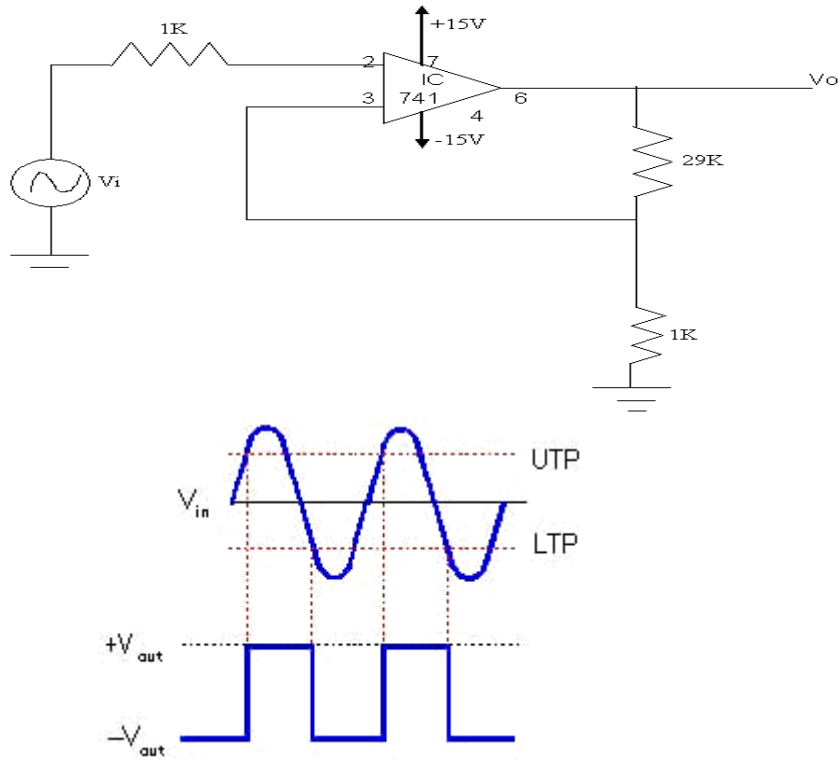
b) **Wien bridge Oscillator:**
1. Design the oscillator for desired frequency using equations
2. Connect the circuit as per the circuit diagram in figure
3. Connect the output of the oscillator to CRO
4. Adjust the POT Rf in feedback loop so that the output is a sine wave.
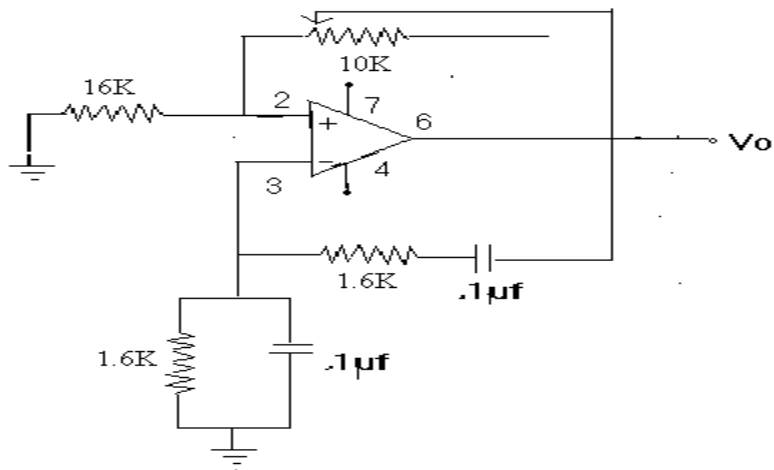5. Plot the output in a graph.
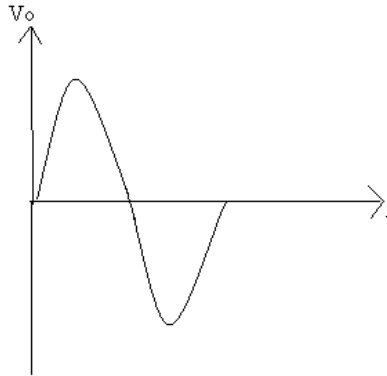
PIN DIAGRAM:
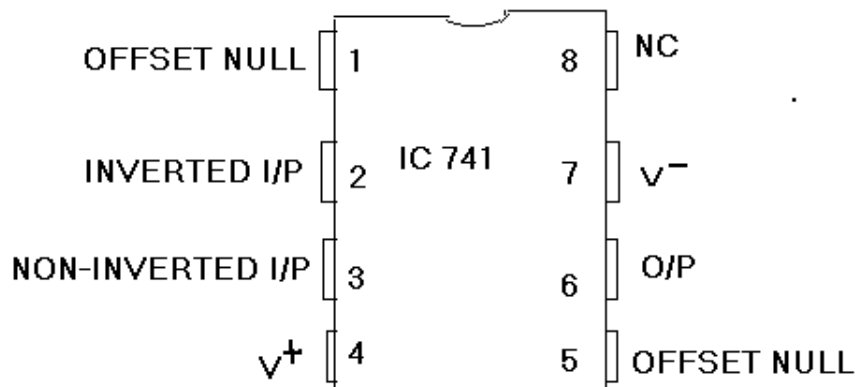
CIRCUIT DIAGRAM:
a) Schmitt Trigger:

	INPUT		OUTPUT	
S.No:	Vin (V)	Time (msec)	Vout(V)	Time (msec)
1.	20	20	28	20

b) Wien Bridge Oscillator:

Vo

t

S.No:	OUTPUT		Theoretical Frequency(Hz)	Practical Frequency(Hz)
	Vin (V)	Time (msec)		
1.	20	0.6	1.5K	1.7K

RESULT:

     Thus Schmitt trigger and Wien bridge oscillator were designed and their operations were studied.

Post Lab Questions:

1.   **How can you obtain triangular wave using schmitt trigger?**

The output of Schmitt trigger when connected to integrator yields triangular output.

2.   **Wein bridge oscillator uses positive and negative feedback. Why?**

Negative feedback is used for stability gain positive feedback is used for oscillation

3.   **What is the function of lead-lag network in Wein bridge oscillator?**

The function of lag lead network is to obtain the zero degree phase shift.

4.   **Why Schmitt trigger is called regenerative comparator?**

The reference voltages LTP andUTP are regenerated depending on the output voltages +Vsat and −Vsat.

5.   **What is hysteresis voltage in Schmitt trigger?**

The difference in voltage between lower and upper threshold voltage is called hysteresis voltage**.**

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S.No:	Marks split up	Maximum Marks (50)	Marks Obtained
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7. Counters

Pre Lab Questions:

1.   What are Counters and what are its types?

A sequential circuit that goes through a prescribed sequence of states upon the application of input pulses is called counter.
- a)   Asynchronous counters
- b)   Synchronous counters.

2.   What are Ripple counters?

Counters in which first flip flop output transition serves as trigger   for the other consecutive flip flops.

3.   What are synchronous counters?

Counters in which clock pulses of all the flip flops are triggered at the same instant.

4.   State the advantage of synchronous counter over asynchronous counters?

Synchronous counter reduces the delay time as all the clock pulses are given simultaneously.

5.   When two counters are cascaded, the overall MOD number is equal to the <u>product</u> **of their individual MOD numbers**.

7. COUNTERS

AIM:

To construct a 4-bit asynchronous and synchronous counters.

APPARATUS REQUIRED:

| S.No	Name of the Apparatus	Range	Quantity
1.	Digital IC trainer kit		1
2.	Connecting wires		As required

.

THEORY:

Asynchronous counter are those in which clock pulse is given to the first flip-flop and the flip-flop output transition serves as a source for triggering other flip-flops. The flip-flops changes one at a time in rapid succession, and the signal propagates through the counter in a ripple fashion. Asynchronous decade counter is also called as ripple counter. In a ripple counter the flip flop output transition serves as a source for triggering other flip flops. In other words the clock pulse inputs of all the flip flops are triggered not by the incoming pulses but rather by the transition that occurs in other flip flops. The term asynchronous refers to the events that do not occur at the same time. With respect to the counter operation, asynchronous means that the flip flop within the counter are not made to change states at exactly the same time, they do not because the clock pulses are not connected directly to the clock input of each flip flop in the counter. Synchronous counters are those in which simultaneous clock pulses are given to all the flip-flops.

PROCEDURE:

1. Connect the circuit as per the circuit diagram.
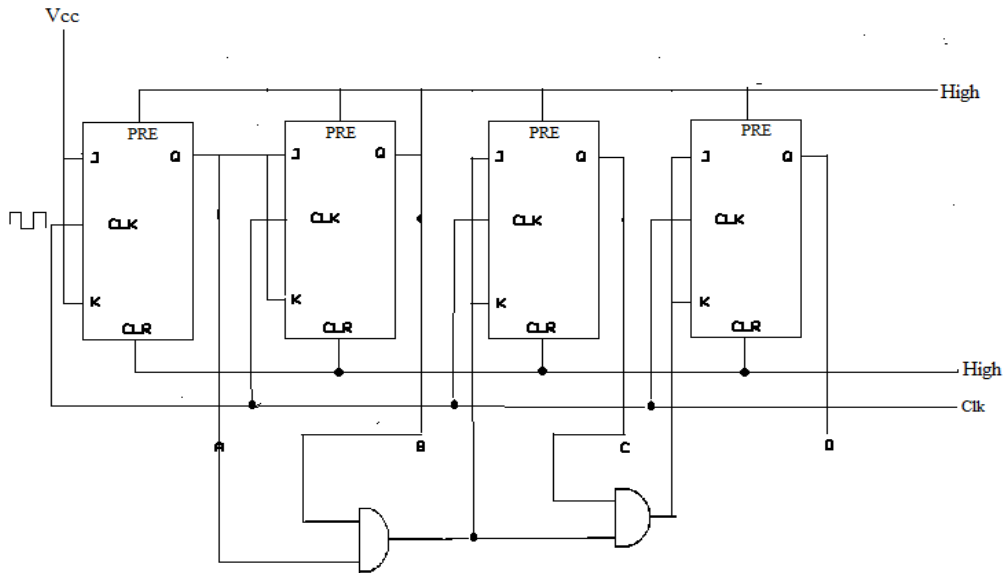2. Note the output and verify the counter operation.

CIRCUIT DIAGRAM:

Asynchronous Ripple counter
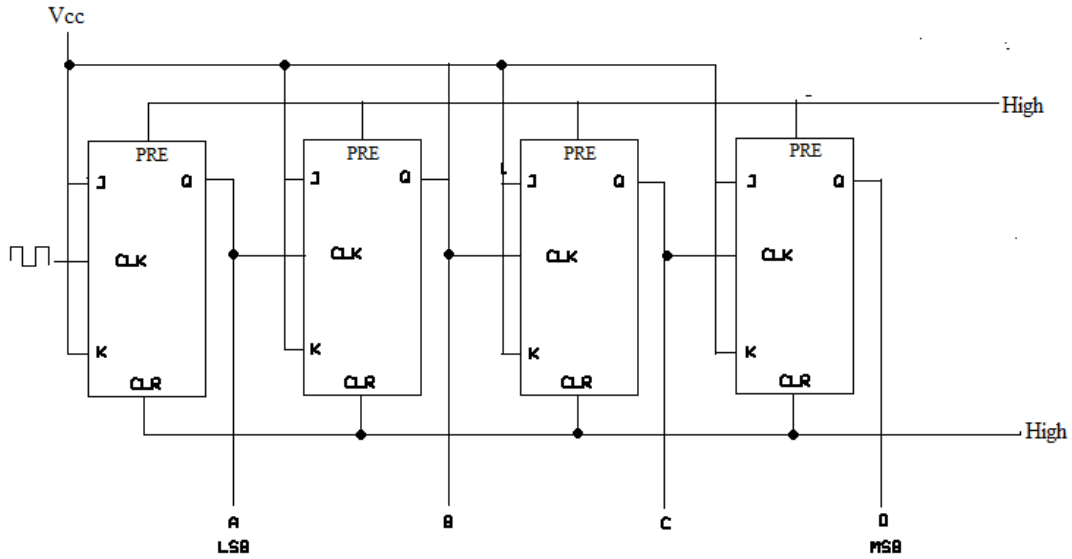
TRUTH TABLE:

A	B	C	D
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

Synchronous Ripple counter:

TRUTH TABLE

A	B	C	D
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

RESULT:

Asynchronous and synchronous counters were designed and truth table verified.

63

Post Lab Questions:

1. **How many flip-flops are required to construct a decade counter?**

   Four (4).

2. **What is MOD counter?**

   The modulus of a counter is the number of different logic states it goes through before it comes back to the initial stage to repeat the count sequence.

3. **How many different states does a 3-bit asynchronous counter have?**

   Eight (8).

4. **State some applications of counters**.

   a) Traffic signals
   b) Medical instruments

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8. Active Filters

Pre Lab Questions:

1.   **What is a filter?**

A filter is a frequency selective circuit that passes a specified band of frequencies and blocks a specified the frequencies outside the band.

2.   **State the advantage of active filters over passive?**

a) Gain and frequency adjustment flexibility
b) No loading problems
c) Low cost
d) Absence of inductors makes the circuit work for high frequency applications.

3.   **Define order of a filter?**

The number of RC networks employed in filter circuits represents the order of the circuit.

4.   **What are the types of active filters?**

a) Low pass filter
b) High pass filter
c) Band pass filter
d) Band reject filter.

5.   **What is frequency response?**

The variation of gain in decibels with respect to frequency is called frequency response.

8. ACTIVE FILTER DESIGN

AIM:

To demonstrate the use of op-amp as low pass and high pass filter.

APPARATUS REQUIRED:

S.No.	APPARATUS	TYPE	RANGE	QUANTITY
1)	Op-Amp	µA741		1
2)	Resistors		29K, 1K, 16K, 1.6K	1
3)	Capacitors		0.1µF	1
4)	Signal Generator			1
5)	CRO			1
6)	Dual power supply			1
7)	Bread Board			1
8)	Connecting wires			

THEORY:

A frequency selective circuit that passes electric signals of desired band of frequencies and attenuates the other band of frequencies outside the band is called an electric filter. At radio frequencies, inductors become problematic. Hence RC filters are used. As op-amp is used in non-inverting mode, it offers high input impedance and low output impedance. This improves the load driving capacity. The most commonly used filters are low pass filter (LPF), high pass filter (HPF), band pas filter (BPF), band stop filter (BSF). Low pass filter passes signals whose frequency is less than cut-off frequency. High pass filter passes signals whose frequency is greater than cut-off frequency. Depending upon the number of RC networks used in the circuit, filters are classified as first order filter if the network contains one RC network and as second order if it contains two RC networks.

DESIGN:

$$f_c = (1/2\Pi RC)$$
f_c - cut-off frequency

PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Give the sine input through the function generator at 1kHz.
3. Observe the output in the CRO for various frequencies.
4. Calculate voltage gain and plot the graph between voltage gain and frequency.
5. Draw 3dB line to determine the cut-off frequency and verify it with the design frequency.
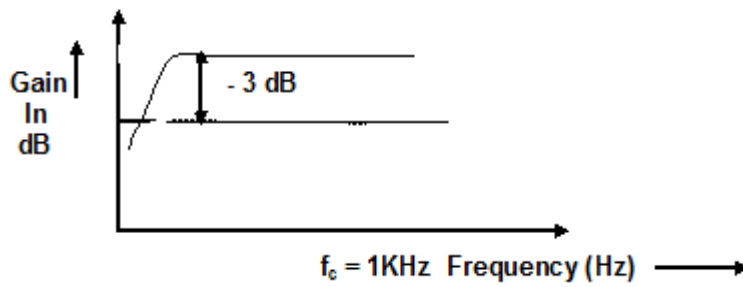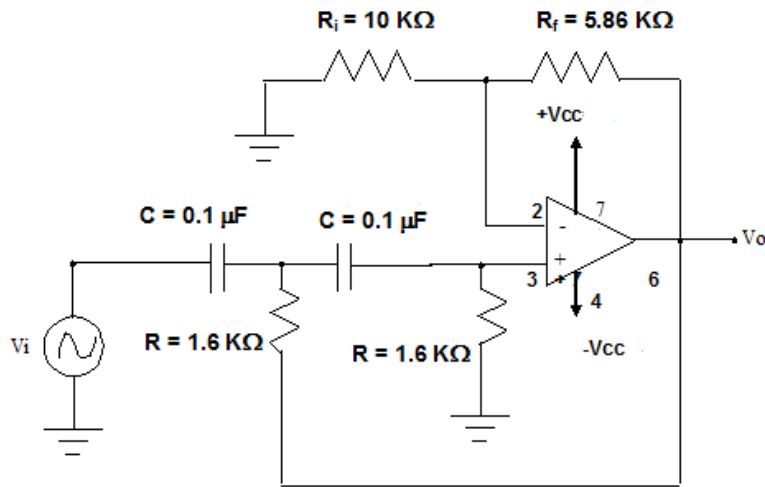
PIN DIAGRAM:
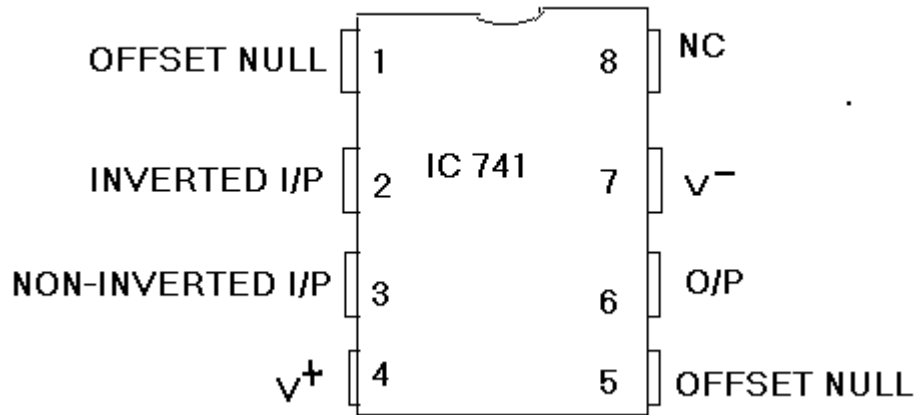
CIRCUIT DIAGRAM:

Second Order LPF:
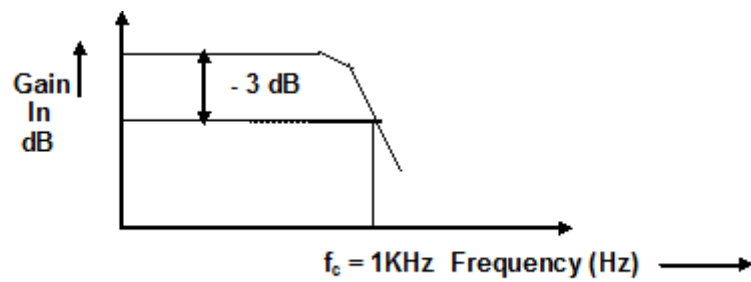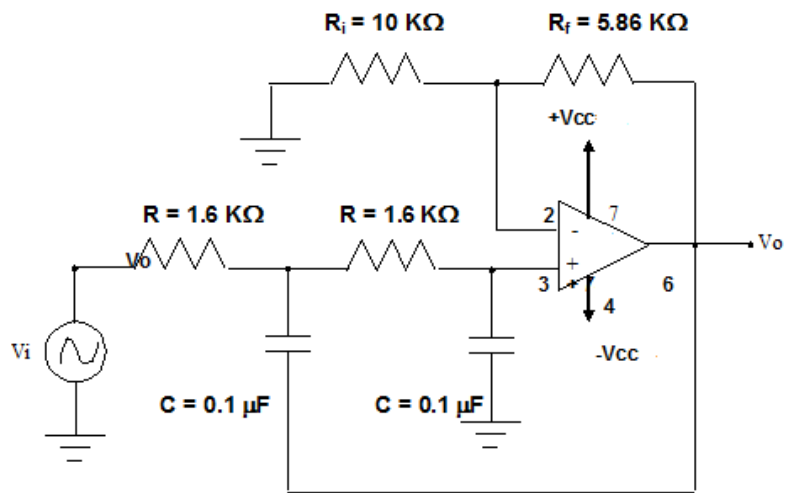
Vin = 2V

S.No.	FREQUNCY (Hz)	O/P VOLTAGE V_O (V)	GAIN Av=20 log Vo/Vi (dB)
1.	800	1	-6.02
2.	850	1	-6.02
3.	900	1	-6.02
4.	1000	1	-6.02
5.	1200	0.9	-6.93
6.	1700	0.7	-9.11
7.	2000	0.6	-10.45
8.	2500	0.5	-12.04
9.	4000	0.4	-13.97
10.	5000	0.3	-16.47

Second Order HPF:

Vin = 2V

S.No.	FREQUNCY (Hz)	O/P VOLTAGE V_O (V)	GAIN Av=20 log Vo/Vi (dB)
1.	800	1	-6.02
2.	1000	1.1	-3.19
3.	1500	1.2	-4.43
4.	2000	1.3	-3.74
5.	2500	1.4	-3.09
6.	3000	1.5	-2.49
7.	3500	1.6	-1.93
8.	8500	1.8	-0.915
9.	9000	1.8	-0.915
10.	10000	1.8	-0.915

RESULT:

The first order and second order low pass and high pass filters were studied.

Post Lab Questions:

1. **Determine the type of filter and the corresponding cut-off rate.**
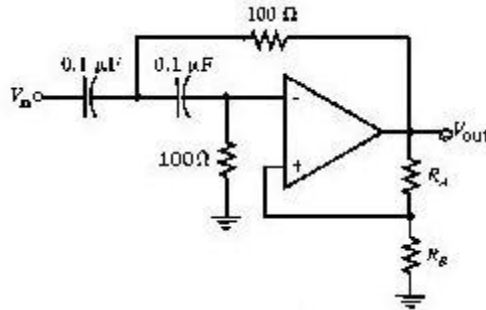
High pass filter, fc = 15.9KHz

2. **What is the significance of 3 db line in frequency response?**

Rms value of sine wave = 0.707
20 log(0.707) = -3db.
The 3 db line gives the cut off frequency.

3. **What are the applications of filters?**

    a) Communication circuits
    b) Transmission

4. **What is state variable filter?**

The State Variable filter has the unique characteristic of producing low pass, high pass, band pass (and notch) outputs simultaneously.

5. **How do you classify active filters based on damping ratio?**

    a) Chebyshev
    b) Butterworth
    c) Bessel.

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9. 555 Timer

Pre Lab Questions:

1.   Give th pin diagram of 555 timer IC.
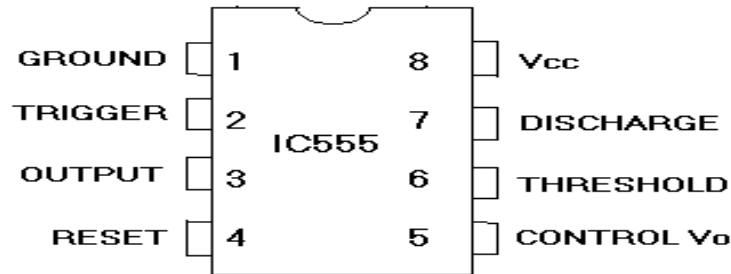
2.   What is multivibrator?

A multivibrator is an electronic circuit used to implement a variety of simple two-state systems such as oscillators, timers and flip-flops. It is characterized by two amplifying devices (transistors, electron tubes or other devices) cross-coupled by resistors or capacitors.

3.   What is quasi stable state?

Change from one state to another without any external trigger is termed as quasi stable state.

4.   What are the various modes of operation of multivibrator? Explain

Astable mode – 2 quasi stable state
Monostable – 1 quasi and on stable state.
Bistable – 2 stable states.

5.   What is one-shot multivibrator?

The monostable is also called as one-shot multivibrator as it produces a single pulse of specified duration in response to each external trigger signal. Only one stable state exists. When an external trigger signal is applied the output changes its state.

9. ASTABLE MULTIVIBRATOR

AIM:

To study the application of IC555 as an astable multivibrator.

APPARATUS REQUIRED :

S.NO	APPARATUS	RANGE	QUANTITY
1)	IC	NE555	1
2)	Resistor	1KΩ, 2.2KΩ	1
3)	Capacitor	0.1μF, 0.01μF	1
4)	CRO	-	1
5)	RPS	DUAL(0-30) V	1
6)	Connecting Wires		

THEORY:

The IC555 timer is a 8 pin IC that can be connected to external components for astable operation. The simplified block diagram is drawn. The OP-AMP has threshold and control inputs. Whenever the threshold voltage exceeds the control voltage, the high output from the OP −AMP will set the flip-flop. The collector of discharge transistor goes to pin 7. When this pin is connected to an external trimming capacitor, a high Q output from the flip flop will saturate the transistor and discharge the capacitor.

When Q is low the transistor opens and the capacitor charges. The complementary signal out of the flip-flop goes to pin 3 and output. When external reset pin is grounded it inhibits the device. The on − off feature is useful in many application. The lower OP-AMP inverting terminal input is called   the trigger because of the voltage divider. The non-inverting input has a voltage of +Vcc/3, the OP-Amp output goes high and resets the flip flop.

The output frequency is,

$$f = 1.44/(R_A + R_B)C$$

The duty cycle is,

$$D = R_B / (R_A + 2R_B) * 100\%$$

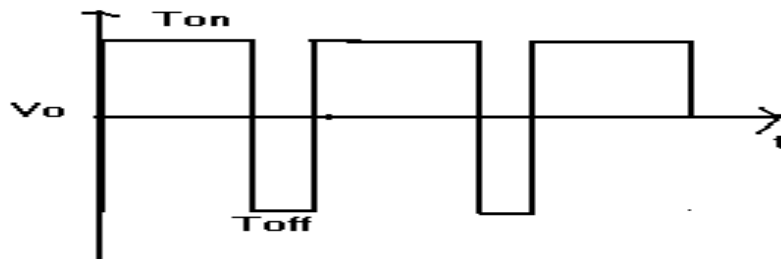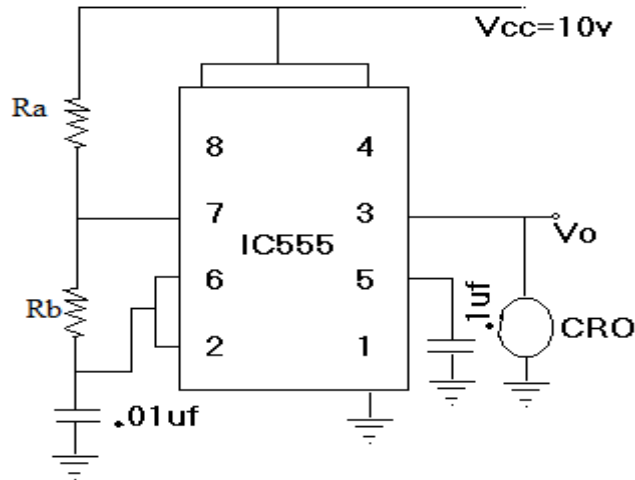The duty cycle is between 50 to 100% depending on R_A and R_B.

PROCEDURE:

1.   The connections are made as per the circuit diagram and the values of R and C are calculated assuming anyone term.

2.   The output waveform is noted down and graph is drawn and also the theoretical and practical time period is verified.

PIN DIAGRAM:
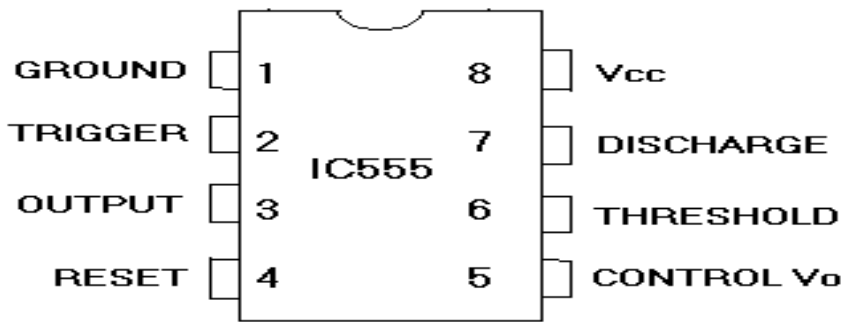
CIRCUIT DIAGRAM:

RESULT:

Thus the astable multivibrator circuit using IC555 is constructed and verified its theoretical and practical time period.

Post Lab Questions:

1. **List the basic blocks of IC 555 timer?**

   - A relaxation oscillator.
   - R-S flip-flop
   - Two comparators
   - Discharge transistors.

2. **Give the applications of 555-timer Astable multivibrator**.

   a) Square wave generator
   b) Voltage Controlled Oscillator (VCO)
   c) FSK Generator
   d) Schmitt trigger.

3. **What is the advantage of 555 IC over op amp?**

   555 IC generates accurate time delay compared to op amp.

4. **List the applications of monostable mode of 555 timer. .**

   a) Missing Pulse detector
   b) Linear ramp generator
   c) Frequency divider

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10. DAC and ADC

Pre Lab Questions:

1.   List all the types of DAC.

      a) Weighted resistor
      b) R-2R ladder
      c) Inverted R-2R ladder.

2.   What is the advantage of R-2R ladder over weighted resistor?

      In weighted resistor, for higher order conversion the values of resistors become very high which is overcome in R-2R ladder which has only R and 2R values of resistors.

3.   List the various types of ADC.

  i) Direct type
      a) Flash type
      b) Counter
      c) Successive Approximation Register
      d) Tracking

  ii)   Integrating type
      a) Charge balancing
      b) Integrating

4.   Define resolution.

Smallest change in voltage which may be produced at output of the converter.

5.   List the specifications of DAC and ADC.

      a) Resolution
      b) Linearity
      c) Accuracy
      d) Monotonicity
      e) Settling time
      f) Stability.

10. DAC and ADC

AIM:

To study the operation of
   i) R-2R DAC
   ii) Weighted Resistor DAC

APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	QUANTITY
1)	IC	μA741	1
2)	Resistor	1KΩ, 2KΩ	1
4)	Multimeter	-	1
5)	RPS	DUAL(0-30) V	1
6)	Connecting Wires		

THEORY:

In weighted resistor type DAC, op-amp is used to produce a weighted sum of digital inputs where weights are produced to weights of bit positions of inputs. Each input is amplified by a factor equal to ratio of feed back resistance to input resistance to which it is connected.

$$V_{OUT} = -R_{F}/R \ (D_3 + 1/2 \ D_2 + 1/4 \ D_1 + 1/8 D_0)$$

The R-2R ladder type DAC uses resistor of only two values R and 2R. The inputs to resistor network may be applied through digitally connected switches or from output pins of a counter. The analogue output will be maximum, when all inputs are of logic high.

$$V = -R_f/R \ (1/2 \ D_3 + 1/4 D_2 + 1/8 D_1 + 1/16 D_0)$$

In a 3 input ADC, if the analog signal exceeds the reference signal, comparator turns on. If all comparators are off, analog input will be between 0 and V/4. If C1 is high and C2 is low input will be between V/4 and V/2. If C1 and C2 are high and C3 is low input will be between 3V/4 and V.

PROCEDURE:
1.   Connect the circuit as shown in circuit diagram.
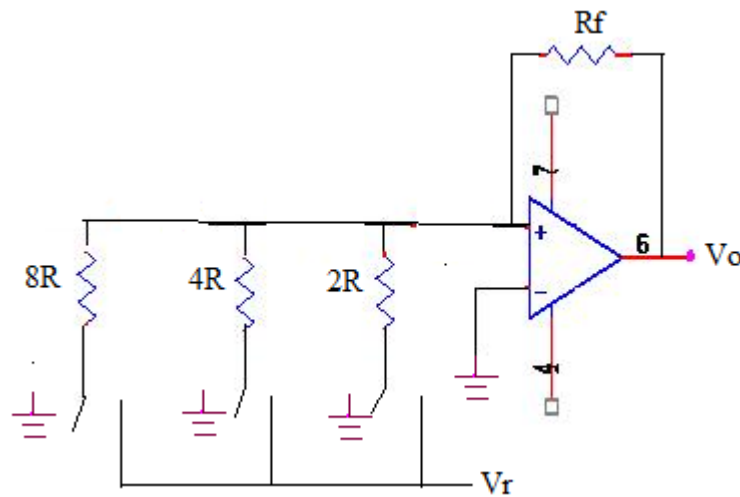2.   For various inputs, measure the outputs using multimeter.
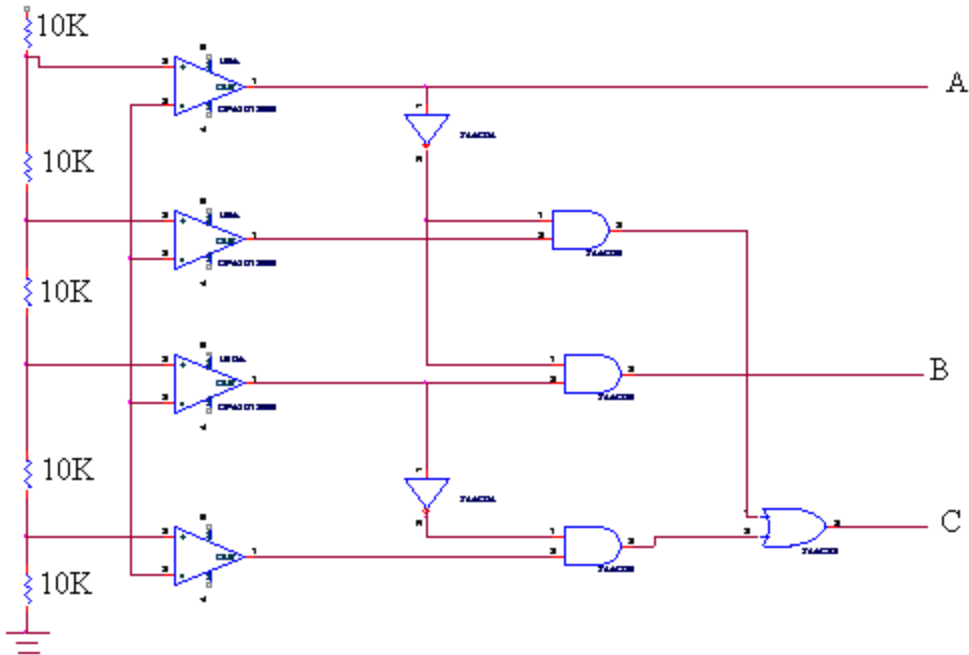
CIRCUIT DIAGRAM:
a) R-2R Ladder DAC:
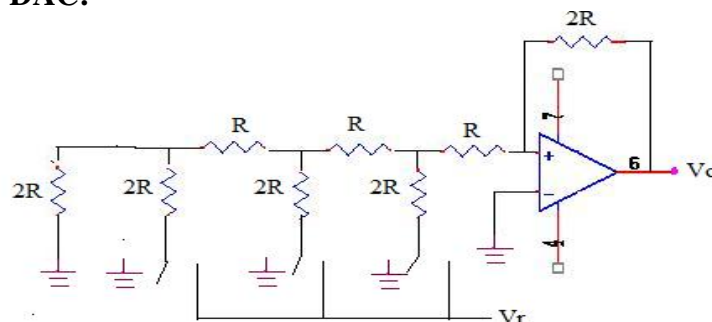
S.No.	D2	D1	D0	Vth	Vprac
1)	0	0	0	0	0
2)	0	0	1	1.25	1.3
3)	0	1	0	2.5	2.7
4)	0	1	1	3.75	3.5
5)	1	0	0	5	4.9
6)	1	0	1	6.25	6.5
7)	1	1	0	7.5	7.2
8)	1	1	1	8.75	8.3

b) Weighted Resistor DAC:

S.No.	D2	D1	D0	Vth	Vprac
1)	0	0	0	0	0
2)	0	0	1	1.25	1
3)	0	1	0	2.5	2.21
4)	0	1	1	3.75	3.22
5)	1	0	0	5	4.62
6)	1	0	1	6.25	5.6
7)	1	1	0	7.5	6.8
8)	1	1	1	8.75	8.1

S.No:	ANALOG INPUT	DIGITAL OUTPUT		
		A	B	C
1)	0-1	0	0	0
2)	1-2	0	0	1
3)	2-3	0	1	0
4)	3-4	0	1	1
5)	4-5	1	0	0

RESULT:

      The operation of R-2R ladder, Weighted resistor DAC and ADC was studied.

81

Post Lab Questions:

1. **How many comparisons will be performed in an 8 bit successive approximation type ADC?**

   8 Comparisons

2. **The basic step of 9 bit DAC is 10.3mV. If 000000000 represents 0V. What output is produced if the input is 101101111?**

   7.38mV.

3. **State the applications of DAC and ADC .**

   a) Digital signal processing
   b) Communication circuits

4. **For R-2R ladder 4 bit type DAC find the output voltage if digital input is 1111. Assume VR = 10V, R = Rf = 10K.**

   Vo = 9.375V

5. **Which is the fastest type of ADC? Why?**

   Successive approximation is the fastest type of ADC. It completes n-bit conversion in n clock periods.

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11. Phase locked loop

Pre Lab Questions:

1.   What is phase locked loop?

It is a circuit which provides frequency selective tuning and filtering without coils or inductors.

2.   List the components of the block diagram of PLL.

      a) Phase detector
      b) Low pass filter
      c) Error amplifier
      d) Voltage controlled Oscillator.

3.   What is voltage controlled oscillator?

Oscillator circuit in which the frequency of oscillations can be controlled by an externally applied voltage.

4.   Define pull in time.

The total time taken by the PLL to establish lock.

11. PLL CHARACTERISTICS

AIM:

　　To construct and study the operation of PLL IC 565 and determine its characteristics.

APPARATUS REQUIRED:

S.No	APPARATUS	RANGE	QUANTITY
1	IC 565	-	1
2	Resistors	6.8 KΩ	1
3	Capacitors	0.001 µF 0.1 µF, 1 µF	1 each
4	FunctionGenerator (Digital)	1 Hz – 2 MHz	1
5	C.R.O	-	1
6	Dual Power Supply	0- 30 V	1

THEORY:

　　A **phase-locked loop** or **phase lock loop** (PLL) is a control system that tries to generate an output signal whose phase is related to the phase of the input "reference" signal. It is an electronic circuit consisting of a variable frequency oscillator and a phase detector. This circuit compares the phase of the input signal with the phase of the signal derived from its output oscillator and adjusts the frequency of its oscillator to keep the phases matched. The signal from the phase detector is used to control the oscillator in a feedback loop. Phase-locked loops are widely used in radio, telecommunications, computers and other electronic applications. They may generate stable frequencies, recover a signal from a noisy communication channel, or distribute clock timing pulses in digital logic designs such as microprocessors

PROCEDURE:

1. The connections are given as per the circuit diagram.
2. Measure the free running frequency of VCO at pin 4, with the input signal V_i set equal to zero. Compare it with the calculated value = $0.25 / (R_T C_T)$.
3. Now apply the input signal of 1 V_{PP} square wave at a 1 KHz to pin 2. Connect one channel of the scope to pin 2 and display this signal on the scope.
4. Gradually increase the input frequency till the PLL is locked to the input frequency. This frequency f1 gives the lower end of the capture range. Go on increasing the input frequency, till PLL tracks the input signal, say ,to a frequency f2.This frequency f2 gives the upper end of the lock range. If input frequency is increased further, the loop will get unlocked.

5. Now gradually decrease the input frequency till the PLL is again locked. This is the frequency f3, the upper end of the capture range. Keep on decreasing the input frequency until the loop is unlocked. This frequency f4 gives the lower end of the lock range.

6. The lock range Δf_L = (f2 − f4).Compare it with the calculated value of ± 7.8fo/12 .Also the capture range is Δf_c = (f3 − f1).Compare it with the calculated value of capture range.

PIN DIAGRAM:
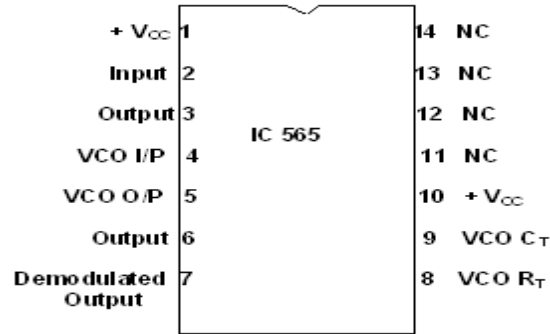
CIRCUIT DIAGRAM:
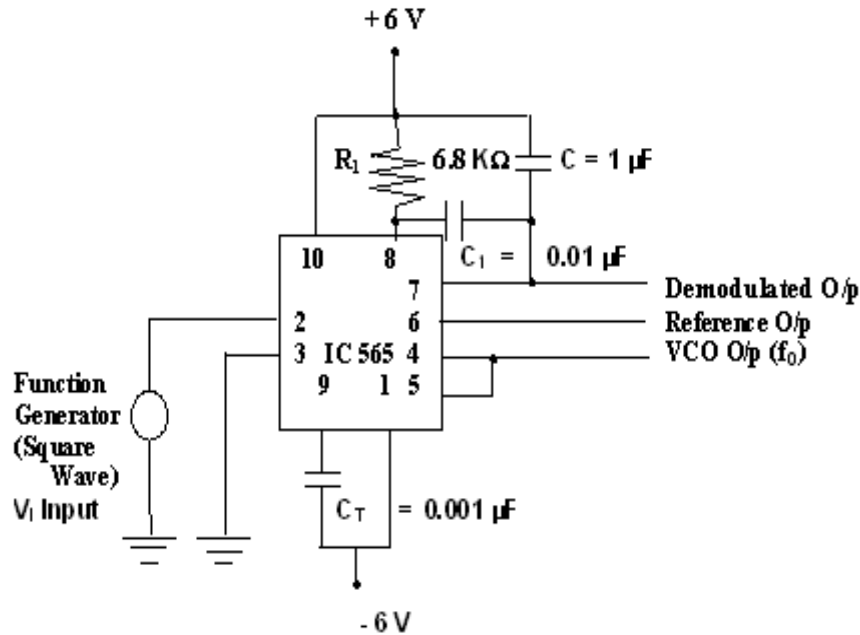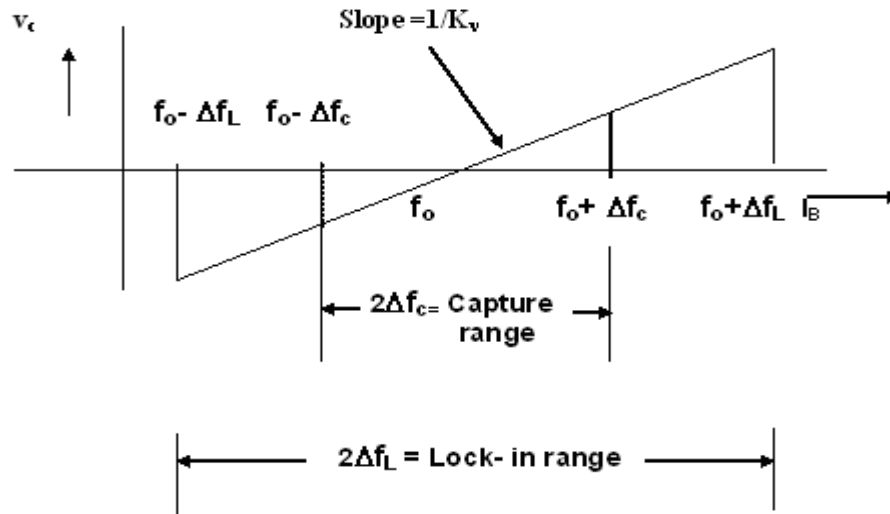
RESULT:

Thus the PLL circuit is constructed and its Characteristics were determined.

87

Post Lab Questions:

1. **Define Lock-in range.**

   The range of frequencies over which PLL can maintain lock with the incoming signal.

2. **Define capture range.**

   The range of frequencies over which PLL can acquire lock with the input signal.

3. **What are the applications of PLL?**

   a) FM Modulation
   b) Signal generation
   c) Frequency shift keying
   d) Frequency multipliers

4. **What are the 3 stages of PLL characteristic?**

   a) Free running
   b) Capture
   c) Locking.

DEPT. OF ELECTRICAL & ELECTRONICS ENGINEERING
SRM UNIVERSITY, Kattankulathur – 603203.

Title of Experiment	:
Name of the candidate	:
Register Number	:
Date of Experiment	:
Date of submission	**:**

S.No:	Marks split up	Maximum Marks (50)	Marks Obtained
1	Attendance	5	
2	Preparation of observation/record	10	
3	Pre viva questions	5	
4	Execution of experiment	15	
5	Calculation/evaluation of result	10	
6	Post viva questions	5	

Staff Signature

12. Voltage Regulator

Pre Lab Questions:

1. **What is a voltage regulator?**

    A voltage regulator is an electronic circuit that provides a stable DC voltage independent of the load current, temperature and AC line voltage variations.

2. **What is the main function of voltage regulator?**

    The main function of a voltage regulator is to provide a stable DC voltage for processing other electronic circuits.

3. **What are the different types of voltage regulators?**

    a)   Fixed output voltage regulator (positive or negative)
    b)   Adjustable output voltage regulators (positive or negative)
    c)   Switching regulators.
    d)   Special regulators.

4. **What are switching regulators?**

    Regulators which operate the transistor as a high frequency ON/OFF switch, so that the power transistor does not conduct current continuously is called switching regulator.

5. What are the four main parts of voltage regulators?

    a)   Reference voltage circuit
    b)   Error amplifier
    c)   Series pole transistor
    d)   Feedback Network.

12. VOLTAGE REGULATOR USING OP-AMP

AIM:
        To design a high current, low voltage and high voltage linear variable dc regulated power supply and test its line and load regulation.

APPARATUS REQUIRED:

S.NO	APPARATUS	SPECIFICATION	QUANTITY
1.	Transistors	TIP122,2N3055	1 each
2.	Integrated Circuit	LM723	1
3.	Digital Ammeter	(0 – 10) A	1
4.	Digital Voltmeter	(0 – 20) V	1
5.	Variable Power Supply	(0 – 30) V-2A	1
6.	Resistors	300Ω ,430Ω ,1KΩ ,678KΩ ,67 8Ω 1Ω	1 each 2
7.	Capacitors	0.1μ F,100pF	1 each
8.	Rheostat	(0 – 350) Ω	1

THEORY:
        A voltage regulator is an electrical regulator designed to automatically maintain a constant voltage level. A voltage regulator may be a simple "feed-forward" design or may include negative feedback control loops. It may use an electromechanical mechanism, or electronic components. Depending on the design, it may be used to regulate one or more AC or DC voltages. Load regulation is the change in output voltage for a given change in load current. Line regulation or input regulation is the degree to which output voltage changes with input (supply) voltage changes - as a ratio of output to input change. Active regulators employ at least one active (amplifying) component such as a transistor or operational amplifier. linear regulator is a voltage regulator based on an active device (such as a bipolar junction transistor, field effect transistor or vacuum tube) operating in its "linear region"

PROCEDURE:
Line Regulation:
1.   Give the circuit connection as per the circuit diagram
2   Set the load Resistance to give load current of 0.25A
3   Vary the input voltage from 7V to 18V and note down the corresponding output voltages
4   Similarly set the load current (I_L) to 0.5A & 0.9A and make two more sets of measurements.

91

Load Regulation:
1   Set the input voltage to 10V.
2   Vary the load resistance in equal steps from 350Ω to 5Ω and note down the corresponding output voltage and load current.
3   Similarly set the input voltage (Vin) to 14V & 18V and make two more sets of measurements.

CIRCUIT DIAGRAM:
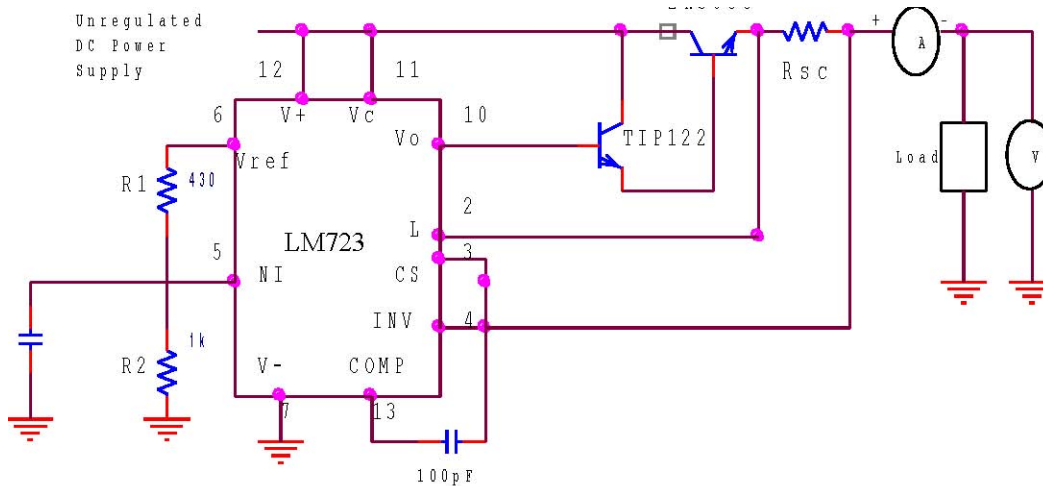
DESIGN:

Vo=5V, Vref = 7.15 V

To calculate R1, R2 ,R3 and Rsc.
Vo = Vref (R2 / (R1 + R2))

$5 / 7.15 = (R2 / (R1 + R2))$

$(R1 + R2) 0.699 = R2$

$0.699 R1 = 0.301 R2$, $R1 = 0.4306 R2$

Select **R2 = 1 K**Ω

R1 = 1 KΩ * 0.4306 = 430Ω

R1 = 430Ω

R3 = R1 * R2 / (R1 + R2) , R3 = 430.6 *1000 /(430.6+1000)

R3 = 300Ω
Rsc = V$_{sense}$ / I$_{limit}$ = 0.5 /1A = 0.5Ω , **Rsc = 0.5**Ω

Load Regulation:

S.No:	I/P Voltage (V)	O/P Voltage (V)
1)	1	5
2)	2	5
3)	3	5
4)	4	4.7
5)	5	4.7
6)	6	4.6

Line Regulation:

S.No:	I/P Voltage	
	O/P Current (mA)	O/P Voltage (V)
1)	1	1.5
2)	2	2.3
3)	3	3.1
4)	4	4.4
5)	5	4.9
6)	6	5
7)	7	5
8)	8	5
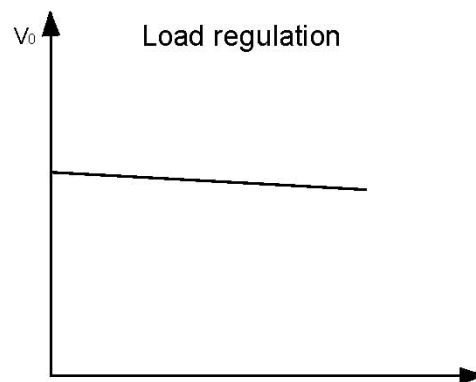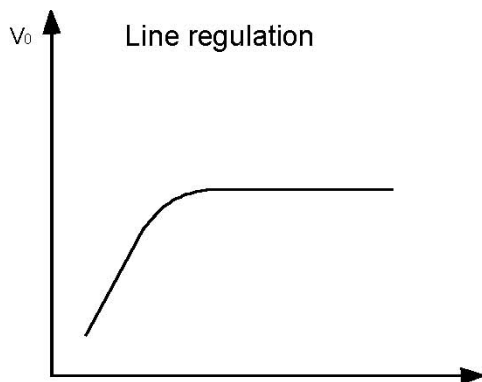
RESULT:

Thus the line and load regulation of low voltage linear variable dc regulated power supply was designed and tested.

Post Lab Questions:

1. **What are the main advantages of voltage regulators?**

   a) Short circuit Protection.
   b) Output Voltage can be varied.

2. **Define line regulation or source regulation.**

   Line regulation is defined as the percentage change in the output voltage for a change in the input voltage. It is usually expressed in millivolts or as percentage of the input voltage.

3. **Define Load regulation.**

   Load regulation is defined as the change in regulated output voltage for a   change in load current. It is usually expressed in millivolts or as a percentage of V_0.

4. **What are the limitations of 723 regulators?**

   a) No built in thermal protection.
   b) It has no short circuit current limits.

5. **What is current limiting ability?**
   Current limiting ability refers to the ability of the regulator to prevent the load current from increasing above a preset value.