VLSI DESIGN RULES

(From *Physical Design of CMOS Integrated Circuits Using L-EDIT*, John P. Uyemura)

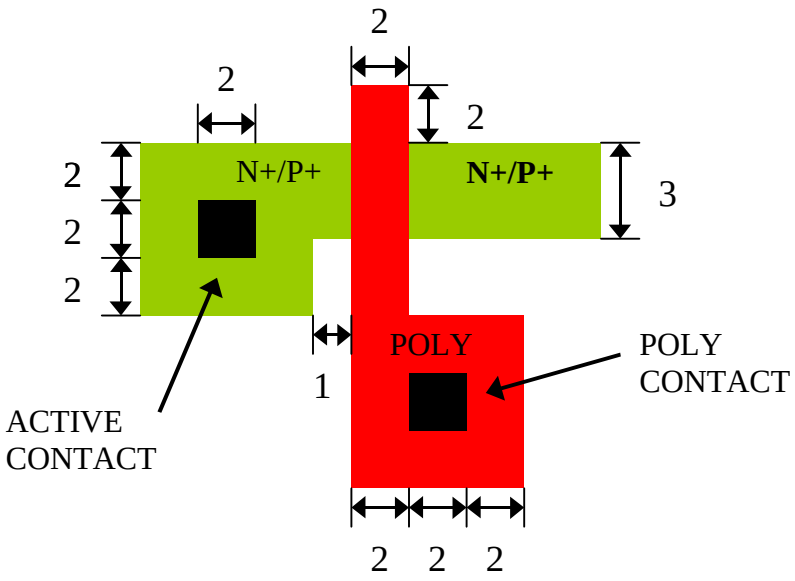
l = 1mm

MINIMUM WIDTH AND SPACING RULES

LAYER	TYPE OF RULE	VALUE
POLY	Minimum Width Minimum Spacing	2λ 2λ
ACTIVE	Minimum Width Minimum Spacing	3λ 3λ
NSELECT	Minimum Width Minimum Spacing	3λ 3λ
PSELECT	Minimum Width Minimum Spacing	3λ 3λ
METAL1	Minimum Width Minimum Spacing	3λ 3λ

MOSFET LAYOUT RULES

RULE	MEANING	VALUE
POLY Overlap	Minimum extension over ACTIVE	2λ
POLY-ACTIVE	Minimum Spacing	1λ
MOSFET Width	Minimum N+/P+ MOSFET W	3λ
ACTIVE CONTACT	Exact Size Minimum Space to ACTIVE Edge	2λ x 2λ 2λ
POLY CONTACT	Exact Size Minimum Space to POLY Edge	2λ x 2λ 2λ

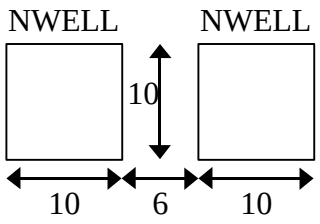


SCNA DESIGN RULE SET

(**S**calable **C**MOS **N**-well **A**nalog)

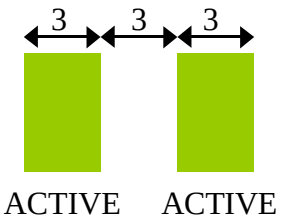
1.0 NWELL

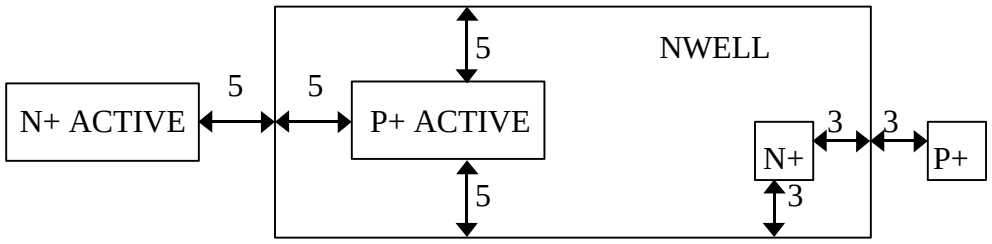
- 1.1 Minimum Width. 10
- 1.3 Minimum Spacing 6



2.0 ACTIVE (N+, P+)

- 2.1 Minimum Width. 3
- 2.2 Minimum Spacing 3
- 2.3 Drain/Source ACTIVE to NWELL
  - 2.3a P+ ACTIVE to NWELL . . 5
  - 2.3b N+ ACTIVE to NWELL. . 5
- 2.4 CONTACT to NWELL EDGE
  - 2.4a P+ in SUB to NWELL. . . 3
  - 2.4b N+ in WELL to NWELL. . 3

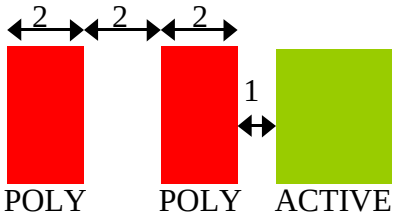


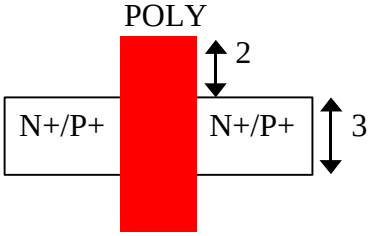


N+ = (NSELECT) AND (ACTIVE)
P+ = (PSELECT) AND (ACTIVE)

3.0 POLY

- 3.1 Minimum Width. 2
- 3.2 Minimum Spacing 2
- 3.3 Gate Extension out of ACTIVE. . 2
- 3.4 Extension (MOSFET)
  - 3.4a nMOSFET Drain/Source . . 3
  - 3.4b pMOSFET Drain/Source . . 3
- 3.5 POLY to ACTIVE Spacing . . . 1





N+ = (NSELECT) AND (ACTIVE)
P+ = (PSELECT) AND (ACTIVE)

4.0 NSELECT and PSELECT

4.2 ACTIVE - SELECT Spacing

4.2a ACTIVE in SELECT . . . 2

4.2b ACTIVE in SELECT to ACTIVE in next SELECT . 2

4.4 Minimum Dimensions

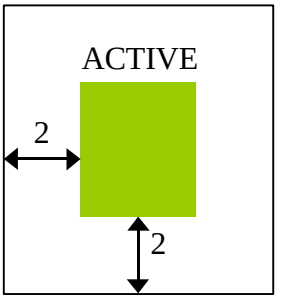
4.4a NSELECT Minimum Width 2

4.4b PSELECT Minimum Width 2

4.4c NSELeCT Minimum Space 2

4.4d PSELECT Minimum Space 2

4.5 PSELECT overlap of NSELECT . 0

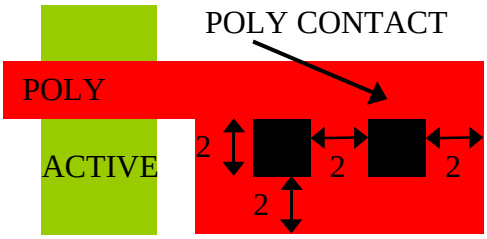


5.0 POLY CONTACT

5.1 Exact Size . . . . . 2 x 2

5.2 Field Poly Overlap of POLY CONTACT. 2

5.3 Spacing 2

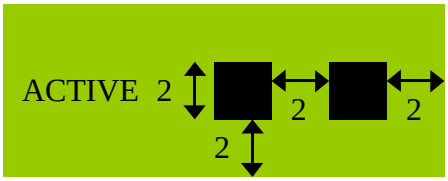


6.0 ACTIVE CONTACT

6.1 Minimum Width. 2

6.2 Field Poly Overlap of POLY CONTACT. 2

6.3 Spacing 2



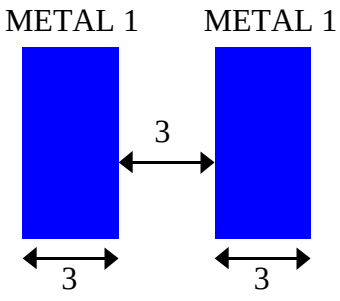
7.0 METAL 1

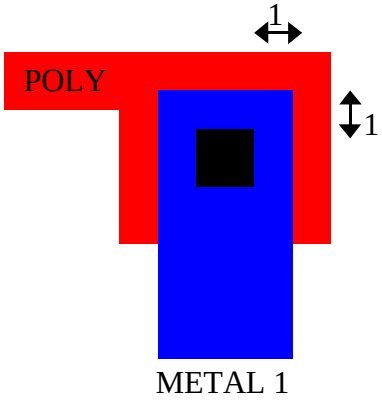
7.1 Minimum Width. 3

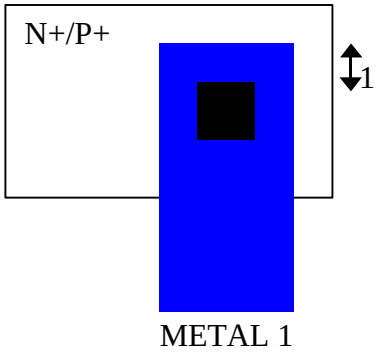
7.2 Minimum Spacing 3

7.3 Overlap of POLY CONTACT . . 1

7.4 Overlap of ACTIVE CONTACT . 1

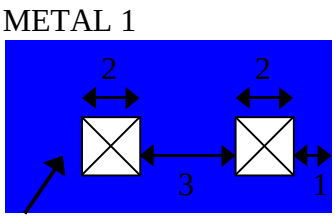






8.0 VIA

- 8.1 Exact Size . . . . . .2 x 2
- 8.2 VIA to VIA Spacing 3
- 8.3 METAL 1 Overlap of VIA. . . . 1
- 8.4 VIA Spacing
  - 8.4a VIA to POLY 2
  - 8.4b VIA (on POLY) to POLY. . 2
  - 8.4c VIA to ACTIVE 2
  - 8.4d VIA (on ACTIVE) to POLY. 2



9.0 METAL 2

- 9.1 Minimum Width. 3
- 9.2 Minimum Spacing 4
- 9.3 Overlap of VIA 4